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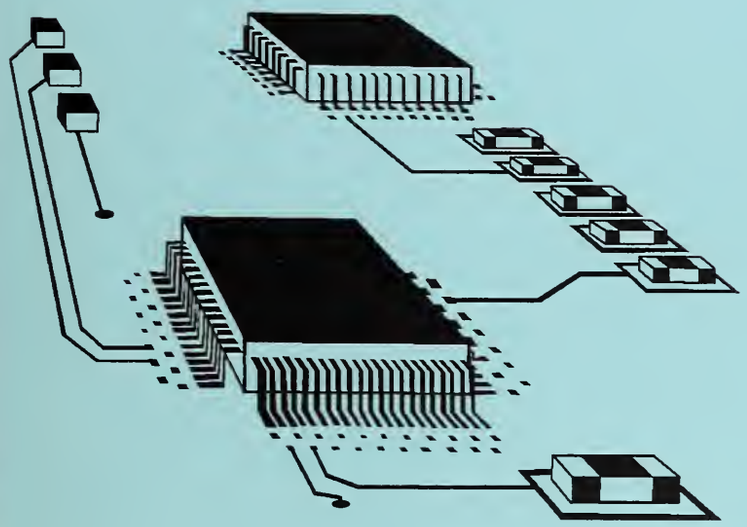

Results of a joint workshop on Materials Metrology and Data for Commercial Electrical and Optical Packaging and Interconnection Technologies

May 5-6, 1994, Gaithersburg, MD.

Edited by Michael A. Schen
National Institute of Standards and Technology

Sponsored by:

NIST

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Institute for Interconnecting and Packaging Electronic Circuits

Optoelectronics Industry Development Association

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November 1994

U.S. DEPARTMENT OF COMMERCE
Ronald H. Brown, Secretary

TECHNOLOGY ADMINISTRATION
Mary L. Good, Under Secretary for Technology

NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
Arati Prabhakar, Director

COVER ILLUSTRATION

Artist's rendition of contemporary electronic packaging and interconnection technologies consisting of J-leaded surface mount quad flat-pack semiconductor packages, chip capacitors, plated through holes and fine-pitch printed wiring board interconnection.

DISCLAIMER

Commercial equipment, instruments, software, materials or services are identified to adequately report the discussions that took place. Such identification does not constitute nor imply recommendation or endorsement by the National Institute of Standards and Technology, the Institute for Interconnecting and Packaging Electronic Circuits, the Optoelectronics Industry Development Association, or the Semiconductor Research Corporation.

FOREWORD

Within industry, government and academia, an awareness exists of the critical role and growing importance of packaging and interconnection technologies for the health and competitiveness of the U.S. semiconductor and printed wiring board, PWB, industries. The plethora of technical symposia and government activities in electronic packaging and interconnection is a testament of this awareness. For policy makers and planners from individual companies, trade associations, research consortia, universities, and government, this awareness signals new opportunities and new challenges for meaningful coordination and cooperation.

In May 1990, the U.S. Department of Commerce, National Institute of Standards and Technology, NIST, held its first workshop in electronic packaging and interconnection. This workshop arose out of NIST's decision to expand its semiconductor microelectronics program to include packaging and interconnection because of the growing impact of these technologies on cost and performance. From this workshop it was concluded that a proper role for the NIST Laboratories was the development of metrology for the measurements of properties of materials and material structures under actual geometries and conditions-of-use. This focus fits well with NIST's historic mission, supports oft-neglected infrastructure needs, is broadly applicable across packaging and interconnection technologies and businesses, and is firmly endorsed by the semiconductor industry. Today, NIST has an expanding program in packaging and interconnection covering polymer, metal, and solder materials.

A number of developments have changed the science, technology, business, and political environments affecting microelectronics since 1990. It is no longer uncommon within industry for technology and business experts to jointly identify future needs, build consensus, and establish research consortia for generic precompetitive technology development. Today, technology "roadmaps" are powerful vehicles for developing action agendas.

The Clinton Administration has made technology policy and civilian technology development key elements of its economic strategy. These include building partnerships; providing additional Federal resources for dual-use and civilian technology development and commercialization through the Technology Reinvestment Project, TRP, and the NIST Advanced Technology Program, ATP; and increasing support for the NIST Laboratory and Manufacturing Extension Partnership, MEP, programs.

The Administration is working to improve the competitiveness of the U.S. electronic packaging industry. This includes a government-funded $30-40 million initiative to stimulate domestic R&D in low cost electronic packaging for high volume applications. Administered through the TRP, the initiative includes the participation of the Departments of Commerce, Energy, and Defense, NASA, and the National Science Foundation.

Though awareness exists of the importance of packaging and interconnection in cost-effective and timely manufacture of electronic products, understandings are still emerging on improvements needed in materials metrology and data by designers, manufacturers, and reliability assessors for creating a quality, robust, and efficient manufacturing environment for the U.S. microelectronics industry. Consequently, NIST and its industry partners teamed together and conducted this second NIST - Industry - University workshop in packaging and interconnection materials metrology and data.

In cooperation with the Institute for Interconnecting and Packaging Electronic Circuits, IPC, the Optoelectronic Industry Development Association, OIDA, and the Semiconductor Research Corporation, SRC, the May 1994 workshop on metrology and data looked at trends, needs, issues, and roadblocks for electrical and optical packaging and interconnection. This report represents the collective views, opinions, and recommendations of over 100 representatives from the materials supply, semiconductor chip manufacturer, and PWB and assembly industries, government and academia who attended this workshop.

The sponsors of this workshop intend this document to be used by planners, administrators, and practitioners from all segments of the U.S. microelectronics and supporting infrastructure industries. Numerous recommendations are proposed. Many of them present challenges on how we conduct business. Nearly all of them require partnerships spanning public-private boundaries and linking supporting disciplines. Certainly all will require time and a great deal of effort. NIST, IPC, OIDA, and the SRC all look forward to working with all segments of industry, government, and academia to implement the findings of this 1994 meeting.

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ABBREVIATIONS and NOTATIONS

APD	Avalanche Photodiode
ARPA	Advanced Research Projects Agency
ASIC	Application Specific Integrated Circuit
ATP	Advanced Technology Program
BGA	Ball Grid Array
C-4	Controlled Collapsed Chip Connection
CAD	Computer Aided Design
CFC	Chloro-Fluorocarbon
CTE	Coefficient of Thermal Expansion
DCA	Direct Chip Attach
DCI	Direct Chip Interconnection
DIP	Dual In-line Package
DOE	Department of Energy
FEA	Finite Element Analysis
FPD	Flat Panel Display
FR	Fiber Reinforced
JPL	Jet Propulsion Laboratories
IC	Integrated Circuit
I/O	Input/Output
IPC	Institute for Interconnecting and Packaging Electronic Circuits
ITRI	Interconnection Technology Research Institute
KGD	Known Good Die
LD	Laser Diode
LED	Light Emitting Diode
MCC	Microelectronics and Computer Technology Corporation
MCM-D	Multichip Module - Dielectric
MCM-L	Multichip Module - Laminate
MCNC	Microelectronics Center of North Carolina
MEP	Manufacturing Extension Partnership
NASA	National Air and Space Administration
NIST	National Institute of Standards and Technology
NVLAP	National Voluntary Laboratory Accreditation Program
OEM	Original Equipment Manufacturers
OIDA	Optoelectronics Industry Development Association
P/I	Packaging and Interconnection
PiN	P-type Semiconductor - Insulator - N-type Semiconductor Photodiode
PTFE	Polytetrafluorethylene
PTH	Plated Through Hole
PWB	Printed Wiring Board
SCM-L	Single Chip Module - Laminate

SNL	Sandia National Laboratories
SEMATECH	SEmiconductor MAnufacturing TECHnology
SIA	Semiconductor Industry Association
SRC	Semiconductor Research Corporation
SRM	Standard Reference Materials
TAB	Tape Automated Bonding
T_g	Glass Transition Temperature
USAF-RL	United States Air Force, Rome Laboratories

ACKNOWLEDGMENT

This two volume NISTIR entitled *Metrology and Data for Microelectronic Packaging and Interconnection* documents the results of a joint Industry - University - Government workshop on "Materials Metrology and Data for Commercial Electrical and Optical Packaging and Interconnection Technologies" conducted on May 5-6, 1994 at the Hilton Hotel in Gaithersburg, MD.

This second workshop on electronic packaging for the U.S. Department of Commerce, National Institute of Standards and Technology, NIST, was conducted on the heels of a number of industry-driven technology "roadmap" exercises and was sponsored by NIST, the Institute for Interconnecting and Packaging Electronic Circuits, IPC, the Optoelectronics Industry Development Association, OIDA, and the Semiconductor Research Corporation, SRC.

Charged with the goal of building a government / industry / university consensus for materials research supporting this technology, NIST is grateful to the many persons and organizations from which valuable insight and guidance was received throughout the planning, conducting, and reporting of this workshop.

Special thanks and gratitude are extended to the Ad Hoc Steering Committee for their many hours spent in teleconferences - either planning, refining, or reviewing workshop goals, agenda, speakers, and reports.

Ad Hoc Steering Committee

Michael A. Schen, Chairman, NIST
Joseph A. Carpenter, Jr., NIST
Carol Handwerker, NIST
George Harman, NIST
David Read, NIST
Arpad Bergh, OIDA
David Bergman, IPC
William T. Chen, IBM
Davis Hartman, Motorola
John Kelly, SRC

NIST and its partners are especially indebted to the industry coordinators and NIST facilitators who shepherded and documented the discussions of the eight technical working groups that met. Their insight and skills were major factors in the success of this exercise.

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Exercises of this nature are only as fruitful as the quality of the people who participate. NIST, the IPC, OIDA, and SRC deeply appreciate the over 100 persons - representing 51 separate organizations including 31 companies and 5 industry consortia - who took part in this public-private planning exercise. Names of speakers and attendees who participated in this workshop are listed in Appendix B of this report. The United States microelectronics and materials industries are indebted to them all.

Michael A. Schen

EXECUTIVE SUMMARY

Michael A. Schen, NIST Polymers

This report on the NIST/OIDA/IPC/SRC Workshop on Materials Metrology and Data for Commercial Electrical and Optical Packaging and Interconnection Technologies identifies cross-cutting barriers, critical technical challenges, and opportunities for NIST in metrology and data for electronic packaging and interconnection technologies. These barriers, challenges, and opportunities are the product of deliberations from eight separate technical working groups that drew upon the insight and experiences of over 100 technical experts from leading U.S. companies in advanced materials, semiconductor, printed wiring board manufacturing and assembly, and interested representatives from academia and government. The technical working groups included:

User-Oriented
- Single Chip
- Multichip Module, Hybrid, and Flat Panel Display
- Printed Wiring Board and Flex
- Electrical and Optical Interconnection and Assembly

Performance-Oriented
- Electrical
- Optical
- Thermal and Mechanical
- Physical, Chemical, and Interfaces

CROSS-CUTTING BARRIERS

While a wide variety of specific barriers and success factors exist in the materials metrology and data that supports the design, manufacture, and reliability assessment of microelectronic products, four cross-cutting barriers emerge that apply to all product applications considered and all technical challenges identified. Successfully surmounting these barriers will substantially add to the rate of progress and competitiveness of U.S. industry. These four cross-cutting barriers are:

In-situ, In-Use, and In-Process Metrology

To improve upon the quality of existing properties data, measurement methods and standards are needed which are specifically tailored for measuring *in-situ* properties of materials, as well as material structures, at the geometries, dimensions, and constraints found in products and processes. Metrology for use in conjunction with manufacturing is a significant contributor to product quality, yield, and development cycle times. The interrelationships between product manufacture and product performance are especially pronounced with polymers. Improved understanding of and data on these relationships are important for new product development and process qualification. For measurements to be useful in a manufacturing environment, tests should be simple, robust and rapid, accurate, and must be correlated to those used during product design and process qualification. Standard test methods need to reflect actual conditions during manufacture. Measurement tools tailored for metal, polymer, and ceramic thin-films and their assemblies are critical for numerous future products.

Data and Databases
Industry strongly needs, and does not yet have, comprehensive thermal, mechanical, chemical, interfacial, electrical, and optical properties data for key packaging and interconnection materials. Such data and databases would enable expanded use of computer aided design and simulation of manufacture and use. The needs encompass data on polymers, metals, and ceramics for substrates, encapsulants, interconnects, and adhesives. Existing databases mostly list properties of bulk specimens which may be significantly different than those at reduced geometries. Data and databases should document characteristics of commercial materials under actual processing, manufacture, and use conditions.

Modeling, Design, and Manufacturing Tools
The lack of integrated and validated modeling tools for design, manufacture, and reliability assessment in packaging and interconnection is a major problem for the electronics industry. Shortened design-cycle-times and time-to-market goals necessitate the development of seamless expert systems for the modeling, design, and virtual manufacture of new products and processes. Increased utility and adoption of these tools hinge upon the availability of comprehensive materials databases, industry-compatible electronic data exchange formats and standards, and model validation and refinement.

Technology Environment
New comprehensive strategies, organizational structures, and leadership organizations are needed in generic technology development, data, and manufacturing to achieve competitive advantages in response to market drivers. This is especially true for the printed wiring board and assembly industry. Reliance on large U.S. companies to lead technology development may be outmoded within the present industrial framework of reduced investments for longer range R&D. Though infrastructure development may be suited for consortia efforts, technology development may be difficult within a consortium framework. Effective coordination and leveraging among existing industry consortia is needed.

CRITICAL TECHNICAL CHALLENGES

Within the context of these four cross-cutting barriers, seven critical technical challenges emerged from the workshop deliberations. These technical challenges strongly impact the performance and reliability of materials and material structures across a wide range of specific engineering solutions in electrical and optical packaging and interconnection. All seven challenges are viewed as high priority areas by industry and require increased attention within industry, university, and government R&D environments. The seven critical technical challenges are:

Adhesion
Surfaces and interfaces are ubiquitous throughout all levels of packaging and interconnection and adhesion is a key concern. Improved fundamental understanding and characterization of surfaces and interfaces are essential for minimizing process variability and improving product reliability. New thin packaging schemes will rely greatly on improvements in adhesion. No standard methods exist for measuring interfaces though numerous standard tests are employed for investigating adhesion. Measurement techniques and standard test structures for characterizing interfaces and adhesion need to be applied to packaging structures where failures occur. Adhesion tests that relate results from stress testing to product delamination are needed.

Moisture Measurement and Control
Moisture-related problems are pervasive in packaging and interconnection and improvements in manufacture and reliability will require improved understanding of moisture effects. Numerous test methods for measuring total moisture exist, however agreement is poor and results often do not relate to product performance. Knowledge of the location and distribution of moisture in complex structures is lacking. Data on volume and mechanical property changes associated with moisture adsorption are unavailable and needed. The role of manufacturing defects in moisture induced failure of interfaces and fracture of encapsulants is unclear. Standards are strongly needed.

Micro Thermo-Mechanical Measurements
Improvements in micro thermo-mechanical measurements and data for specimens with dimensions much smaller than 0.1 mm are needed as feature sizes are reduced. Most existing mechanical properties data are based upon methods and standards established for engineering structures and do no reflect microelectronic applications. Improved standard testing metrology is needed to update existing methods. Advancements in interconnect reliability rely heavily on improved understanding of and data on micro thermo-mechanical properties of metals and polymers. Fatigue, fracture toughness, and stress-strain measurements are among the properties where data are needed.

Dimensional Stability
Improvements in dimensional stability are central to many advanced packaging and interconnection solutions, like BGA substrates, ultra thin packages, and alignment of optical interconnects. New adhesive, encapsulant, and PWB and Flex substrate materials with higher operating temperatures, lower CTE, and lower moisture uptake are one approach to improving dimensional stability. New materials development should strive to utilize existing manufacturing infrastructure to minimize cost. Improved modeling of dimensional response to processing and use conditions are needed. Dimensional metrology, especially with nanometer-scale resolution, and standards are needed to realize cost-effective application of new technologies.

Failure Mechanisms
Current knowledge of failure mechanisms that underlie known failure modes is inadequate as it applies to single chip, multichip module, hybrid, and flat panel display packaging, PWBs and Flex, and optical and electrical interconnection. Delamination, corrosion, electromigration, film defects, dielectric breakdown, popcorning, crack propagation and fracture are some typical examples of failure modes affecting the multilayer packaging structures. Knowledge of and accelerated test methods for true failure modes are needed to improve material selection, design and use.

High Frequency Electrical Measurements
Semiconductor components and assembled systems are operating at ever higher frequencies which is driving developments in high performance packaging. Industry-wide improvements in high frequency (100 MHz-100 GHz) electrical properties are needed for making rational choices as to which technology can provide the required electrical performance and reliability at the lowest cost. Proper electrical characterization and analysis methods are complex and expensive and industry-wide standard testing methods are badly needed. Limited industry expertise in high frequency electrical measurements necessitates improvements in education, training, and dissemination of measurements know-how.

Interconnection
The lack of integrated modeling tools, and the poor cooperation and coordination that typifies current interconnection development practices, hampers product design-cycle-times and reliability. Improvements in the quality of materials tests and data for interconnects will substantially improve the development process. A predictive test of manufacturing solderability for in-line process control, tolerances and measurements for component placement and component lead co-planarity, measurements of intrinsic alignment stability of optical interconnections, feature accuracy for lithographic patterning of optical waveguides, optical properties measurements, interconnect mechanical properties and reliability, and in-line process control are among the priority issues involving materials.

OPPORTUNITIES FOR NIST

Industry strongly endorses NIST's growing involvement in microelectronic packaging and interconnection, and a program that targets the barriers and challenges associated with materials and material structures. Industry also believes NIST could help meet their needs in the following ways.

- **Spearhead the establishment of a national task force on packaging and interconnection metrology and data that brings together key segments of the microelectronics industry, facilitates advancements, coordinates research and disseminates results**
- **Develop fundamental understanding of materials and material structures**
- **Develop and disseminate improved measurement and testing methods for materials and material structures, especially those well suited for the manufacturing environment**
- **Broadly disseminate R&D expertise and results to industry by employing round robins**
- **Develop a standards program that seeks adoption of improved methods by national and international standards bodies, produces standard reference materials and material structures, and develops and tests standards for the electronic exchange of materials data**
- **Conduct with industry an objective assessment of existing industry test standards, new standards needs, and current materials databases**
- **Work closely with industry groups, consortia and standards organizations like SIA, IPC, OIDA, SEMATECH, SRC, ITRI, SEMI, and ASTM.**

INTRODUCTION

Michael A. Schen, NIST Polymers

Integrated circuits and printed circuit boards are the two most strategic and pervasive electronic components which impact the U.S. electronics industry and today's modern life [1]. Semiconductors, electronic packaging and interconnection, and assembly are essential parts of today's $300 billion U.S. electronics industry [2] - an industry that employs more people than the automotive, steel, and aerospace industries combined [3]. PWB manufacturing and PWB assembly alone provides over 200,000 U.S. jobs and accumulates $12 billion in sales annually.

Optoelectronics and photonics are key high-technology enablers for the information and communications revolution now underway. Already well established in long-distance fiber-optic telecommunications and flat-panel display technologies, optoelectronics will play an important role in high density data storage and printing technologies. Optoelectronics in combination with silicon technology promises advances in data bandwidth, access, and display that will enable far more efficient and ergonomic man-machine interfaces. Today's $50 billion world-wide market for optoelectronic equipment is expected to become a $460 billion business by 2013 [4].

As semiconductor technology continues its trend towards reduced cost and improved performance and reliability, it is the packaging and interconnection of the silicon chip that many expect will soon limit system performance and determine product cost. Already packaging represents nearly one-third of the delivered cost of integrated circuits [5]. In optoelectronics products, packaging is the major cost factor for delivered devices - representing as much as 75% in some cases [6]. Demands on packaging extend well beyond the historical function of providing physical protection and electrical or optical connections. Today, packaging provides the link between the semiconductor or optical fab, the materials supplier, and the system-building customer.

Industry Planning and Technology Roadmaps

In November 1992 and June 1994 the Semiconductor Industry Association, SIA, and key semiconductor technologists from across the country convened two landmark workshops to create a common vision for semiconductor technology over the next 15 years [5]. The resulting technology "roadmap" evaluates likely progress and roadblocks in key areas relative to expected industry requirements and identifies how resources might be best used to ensure a vigorous domestic industry in the years to come. Key roadmap recommendations include effective technical partnership between industry and appropriate parts of the government, and an endorsement of NIST's programs in semiconductor metrology. A significant outgrowth of the workshop is SEMATECH's and SRC's decisions to expand their efforts in packaging in 1994.

In December 1992, the Institute for Interconnecting and Packaging Electronic Circuits, IPC, recognized the need to help steer future research and development in the electronic interconnection industry and integrating new technologies into the marketplace. From this, two related developments emerged. First, in April 1993, the IPC assembled leaders from the electronic interconnection industry, their customers and suppliers, and experts from government and academia to develop a "roadmap" for the U.S. interconnection industry [7]. From this, over 150 specific recommendations were developed in materials, assessment methods, manufacturing, quality, reliability, and inspection. To help implement these recommendations, the industry took a second step by establishing the Interconnection Technology Research Institute, ITRI. ITRI's goal is to catalyze formation of research consortia within industry and government, to disseminate new information and technologies to industry, and to focus and leverage current investments in interconnection.

Lastly, the Optoelectronics Industry Development Association, OIDA, conducted a series of workshops in 1992 and 1993 centered about market applications and technology challenges for the emerging optoelectronics industry. NIST, in cooperation with OIDA, explored many of the key materials issues in photonics in the August 1992 Photonic Materials Workshop[8]. The product of OIDA's efforts is the April 1994 *Optoelectronic Technology Roadmap* [4]. This "roadmap" presents a vision of future optoelectronic markets and technologies by the North American optoelectronics industry and of actions needed for the industry to compete globally.

Workshop Strategy

Building on the successes of these planning exercises, the NIST/IPC/OIDA/SRC workshop targeted representatives from small, mid-size, and large U.S. firms representing the semiconductor, printed wiring board, and supporting materials supplier industries. An analysis by sector of workshop registrants is summarized in Table I.

Table I: Workshop Participation

ATTENDANCE		REPRESENTATION	
109 TOTAL REGISTRANTS		51 SEPARATE ORGANIZATIONS	
49 (45%)	Industry	5	Industry Consortia (ITRI, MCC, MCNC, SEMATECH, SRC)
20 (18%)	University	31	Private Firms
40 (37%)	Government	11	Universities
27 (25%)	NIST	5	Government Agencies (ARPA, DOE-SNL, NASA-JPL, NIST, USAF-RL)
13 (12%)	other agencies		

The purpose of the workshop was to augment industrial efforts in three ways.

- Identify priorities in materials data quality, applicability and availability, and the underlying measurement science, for the design, manufacture, and reliability assessment of critical electrical and optical packaging and interconnection materials, structures, and processes.
- Bridge the gap between materials suppliers, device manufacturers, and systems assemblers through coordinated R&D planning.
- Catalyze formation of collaborations and alliances between materials suppliers, microelectronic device manufacturers and users, industry consortia, universities, standards bodies, and NIST for efficient utilization of public and private resources.

This workshop had four very specific goals.

- Interpret the packaging and interconnection goals contained in the semiconductor, printed wiring board and optoelectronic technology roadmaps in light of materials measurement science and data.
- Assess the challenges and priorities of metrology and data presently employed by U.S. industry in the design, manufacture, and reliability assurance of critical electrical and optical packaging and interconnection materials, structures and processes.
- Identify and prioritize advancements needed in materials metrology and data to support industry-stated technology goals.
- Begin the development of a national consensus in materials research and metrology for electrical and optical packaging and interconnection that can be used by planners and administrators from all segments of the U.S. microelectronics industry.

Eight separate working groups met during the two day period. On the first day, four **technology**-focused working groups met to address the challenges and priorities in materials measurement and data to support the design, manufacture, and reliability assessment of critical electrical and optical packaging and interconnection materials, structures, and processes. They included:

- Single Chip
- Multichip Module, Hybrid, and Flat Panel Display
- Printed Wiring Board and Flex
- Electrical and Optical Interconnection and Assembly

These user-oriented working groups were asked to address the **challenges and priorities** in materials metrology and data to support the design, manufacture, and reliability assessment of critical electronic and optical packaging and interconnection materials, structures and processes, and to consider the following questions.

Q1. What is the scope of your working group discussions?
Q2. In light of industry roadmaps, what are the critical packaging and interconnection structures, processes, or materials needed to meet industry goals?
Q3. What design, manufacture, or reliability characteristics are most important?

Q4. What is the status of materials metrology and data quality, data availability, and data applicability used to support these critical elements in design? In manufacture? In reliability assessment?
Q5. What deficiencies exist? What improvements are needed to overcome industry-identified roadblocks?
Q6. What metrology is most needed? What areas are under addressed?
Q7. What data are most important? What gaps exist?
Q8. What standards are most important? What improvements are needed?

From these four technology-focused working groups four preliminary reports were generated that identify and prioritize the critical metrology and data challenges in: a) design; b) manufacture; and c) reliability assessment. These reports were distributed to all the performance-focused working groups.

On the second day, four **performance**-focused working groups met to address the status, challenges, and gaps in metrology and data to describe the properties of materials utilized in the critical packaging and interconnection materials, structures, and processes identified the previous day. The groups included:

- Electrical
- Optical
- Thermal and Mechanical
- Physical, Chemical, and Interfaces

These infrastructure support related working groups were asked to address the **status, challenges, and gaps** in metrology and data to describe the properties of materials utilized in critical electrical and optical packaging and interconnect structures and processes. During their deliberations, the following questions were examined.

Q1. What is the scope of your working group discussions?
Q2. What measurement issues identified during yesterday's discussions are relevant to this working group?
Q3. What is the status of measurement science being utilized to meet industry's identified needs?
Q4. What advanced metrologies are available which could be brought to bear on industry's needs?
Q5. What advancements in measurement science are needed? What are the priorities? Are there road-blocks?
Q6: What advancements in data are needed? What are the priorities? Are there road-blocks?
Q7. What standards are most important? What improvements are needed?
Q8. What are the technical recommendations?
Q9. Are there specific recommendations for NIST? For IPC/ITRI? For OIDA? For SRC?
Q10. Which organizations should be working together? In what areas?

From these two sets of working groups, this final report has been assembled to capture the deliberations, outputs, and recommendations of this industry-led workshop.

PRODUCT DRIVERS

SINGLE CHIP

William T. Chen, IBM Corporation
G. Thomas Davis, NIST Polymers

INTRODUCTION

Single chip packaging is the workhorse of the semiconductor packaging business. In most cases, the users of semiconductor chips buy them from the suppliers packaged in single chip modules. The scope of this working group included most aspects of single chip packaging. While the needs were in both metals and polymers, the emphasis was clearly on problems associated with polymers and the interfaces with polymers. Here, the word polymer encompasses materials such as adhesives for die attach and heat sink attach, molding compounds, encapsulants, underfill, the tape used in tape automated bonding, and the polymer materials used in forming the laminated substrates for SCM-L packaging. Frequently the polymer materials are polymer composites or filled polymers. For example, molding compounds and encapsulants are often more than 50% filled to achieve improved mechanical properties. The importance of the properties of metals used in lead frames, wirebonds, solder joints, and substrate interconnects were also discussed, including the surface metallurgy and characteristics for polymer to metal bonding.

SUMMARY

Principal demands on materials metrology for single chip packages are associated with measurement capability for specific properties in the configuration of use. For example, as a thin polymer layer between die and substrate, filled polymer molded around die and wirebond interconnections, or underfill encapsulants surrounding solder bumps between die and substrates.

Reliable measurement tools for measuring material properties under conditions encountered in processing such as elevated temperature, pressure, and shear flow are important for delivering quality products on time.

Comprehensive databases of material properties to enable design, manufacture, and assembly of electronic packages are strongly needed. These should include properties under in-use conditions and at the temperature, pressure, and shear conditions encountered during manufacturing. Variations in physical properties that can be expected for reasonable variations in processing conditions are included.

Better understanding of surfaces and interfaces is required for design and reliability modeling and improved techniques are needed to easily measure surface properties of materials. Interfaces between dissimilar materials are ubiquitous in electronic packaging. Better insight and tests that relate results from stress testing to delamination encountered in practice are important. A much better understanding of the interactions and role of moisture at interfaces is critical since most device failures are initiated at interfaces.

PARTICIPANTS

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Nick Rounds, Plaskon
Sharad Shah, Digital Equipment Company
Bob Sundahl, Intel
Clare Thiem, USAF-Rome Laboratories

STATUS

Technology Environment

Market forces are driving the manufacture of low cost plastic single chip packages for high I/O applications to thinner, smaller, and more compact form factors. Laminate substrates for single chip modules, SCM-L, with ball grid array will share with plastic packages the industry infrastructure and materials and processes knowledge base. These packaging structures are already drawing on the leading edge capabilities and manufacturing infrastructure of the printed circuit industry for low cost SCM-L with high I/O requirements. The same laminate substrate will meet the needs of chip packages wherever it becomes the most cost effective solution for user needs. The construction of MCM-D relies heavily on the use of photolithographic circuit definition techniques and tools common to IC fabrication. It is reasonable to expect that single chip packages will broaden their capabilities to meet the needs of different industry sectors with plastic packages and SCM-L for most low cost applications.

Physical Design

Comprehensive databases of relevant materials properties for key materials to enable materials selection and design of electronic packages do not exist and are needed. Existing databases generally list properties of bulk specimens which may be significantly different from the properties in the geometry of use such as thin polymer and metal films. Materials such as molding compounds and encapsulants are purchased from specialty materials suppliers, often with little published literature concerning material properties. The CINDAS database is designed to fill this gap but much more work still needs to be done. The variety of materials and the type of relevant properties which should be included are exemplified in the 12th figure of Barry Johnson's presentation (see Volume II, page 7, lower).

A number of software programs are in general use by those who design packages and interconnects but each is rather highly specialized. Programs like AUDiT developed at Cornell University simulate packaging architecture. Programs for placement and routing are available commercially from companies such as Cadence and Mentor Graphics. Additional software packages are available for electrical, thermal and mechanical analysis. Few validations of modeling programs have been demonstrated. This is needed to develop user confidence in the qualitative and quantitative validity of the physics underlying the simulations. Such validation exercises require reliable data of relevant materials properties.

Manufacture and Assembly

Metrology for use in conjunction with manufacturing and assembly tools and processes is a significant contributor to product robustness, yield, and development cycle time; all important factors to global competitiveness. Time consuming research techniques are often required to understand and measure polymer related properties such as fracture toughness of a molding compound or adhesion of two different polymers in a package. For measurements to be useful in a manufacturing environment, simple, robust and rapid tests are required that yield data which can be correlated to those obtained during product design and process qualification. A suggested "rule of thumb" is that such tests should require no more than ten minutes per specimen.

Reliability

The availability of readily accessible, comprehensive, and reliable data on materials properties, especially as a function of temperature, is a critical enabler for the modelling of reliability. Understanding of interfaces and the effects of moisture are especially important. The weak link in packages is often tied to delamination at interfaces and crack initiation in the package, leading to eventual failure.

Electronic packages are generally tested with highly severe stress testing to reveal weak links and associated acceleration factors. Although failure modes have been identified in many cases, failure mechanisms are not known. Models typically predict some materials deformation behavior but models for failure mechanisms, including statistical distributions of materials strength or other failure criteria, are generally required. The materials properties associated with probable failure mechanisms need to be identified in order to accurately assess reliability for the targeted customer use.

CRITICAL MATERIALS, STRUCTURES & PROCESSES

Materials

The trend toward smaller and smaller devices operating at higher and higher frequencies is placing increased demands on the properties of materials. Chip integration, higher frequencies, and the higher power density and compactness of packages for portable design will lead to increases in device junction temperatures. These operating conditions will impact the glass transition temperature requirements of the polymer materials as well as the thermally driven stress in the package. Molding compounds, encapsulants, and underfills which can provide strong interfacial adhesion and good processing windows will be critical to successful and competitive packages.

To take advantage of the higher operating frequencies of the ICs, the dielectric constant of dielectric materials separating signal and ground planes must be reduced to as low a value as practical. Typical ceramic materials exhibit a dielectric constant of 7 to 9, epoxy-glass laminate a little above 4, polyimide sheet or thin film about 3.5 to 4, and pure polytetrafluoroethylene (PTFE) a value near 2. Silica which is often used as filler for molding compounds has dielectric constant near 4.2. In contrast to the low dielectric constant required of dielectric materials, materials with high dielectric constants are desired for decoupling capacitors in the package. High temperature and low dielectric constant laminate packages will be particularly attractive for high performance applications where the traditional epoxy-glass materials capabilities are limited. In addition to materials with the desired physical and processing properties, an infrastructure to manufacture and supply the materials at competitive cost and dependable quality is essential for acceptance by the industry. Lower dielectric loss materials are particularly important for microwave packaging applications.

Some leadframes are now being supplied with new plating surfaces such as palladium and one can expect additional platings and surface preparations to enhance adhesion. These changes in surface metallurgies will impact encapsulant (globtop) and molding compounds to provide appropriate interfacial adhesion.

Availability of robust photosensitive polymer materials for top surface dielectric may give significantly lower cost processing advantages for substrate manufacturing. Anisotropic conductive adhesives would be a highly attractive alternative to solder bumps for flip chip packaging. The properties of these materials have been designed to have process and functional properties widely disparate, and yet have high potential for significant manufacturing cost advantages for specific markets or applications. Metrology for these materials can be expected to be particularly process sensitive.

Structure

Single chip packages come in many different forms, designs, and structures. Materials improvements and innovation have played major roles in developing new structures and designs to lower cost and improve versatility and reliability. It is generally believed that plastic packages will continue to serve most user needs except for the high end and for applications where stringent environmental requirements demand their hermetically sealed counterparts. Laminate packages are emerging to meet the high I/O IC requirements where conventional plastic packages have severe limitations. Ball grid array appears to be the leading candidate for second level assembly attach to the card for high I/O module packages.

As the number of I/O connections to the IC increases for microprocessor and ASICs according to the SIA roadmap projections, the challenge to interconnection technology (design, materials, processes and cost) becomes enormous. Area array flip chip such as C-4 and area array second level attach such as ball grid array, are expected to be the approach. The manner in which new designs and materials such as anisotropic electrically conducting adhesives will be used in this dynamic industry will depend critically upon materials and process advancements and the industry's knowledge about these advancements. Concurrent with the interconnect requirements, there will be wireability requirements to accommodate these high I/O ICs. High wiring density laminate packages will be needed for global wiring interconnections at the card level and local wiring escapes at the module level. Laminate structures based upon materials, processes, and infrastructure of the printed circuit industry will provide the advanced substrates for future high I/O "plastic" packages. These can be expected to evolve from the materials infrastructure of encapsulants, molding compounds, underfill encapsulants, conductive adhesives, heat sink materials and adhesives, flip chip and wirebond interconnects of today's industry.

Processes

Single chip module packages are manufactured in high volume manufacturing processes with high expectations of yield. While wirebonding and solder reflow processes have been developed over a number of years, the demands for size and spacing continue to shrink. Polymers and polymer composites in the form of adhesives and encapsulants and molding compounds provide electrical, thermal, and structural functions to the package. The polymer properties have been tailored to provide the properties to meet those requirements. In the manufacturing process it is crucial to develop process windows and know the influence of process variables on material properties. A database of the materials set must reflect the processing conditions and it must also include expected variations in materials properties with reasonable variations in the processing conditions. For example, an adhesive or encapsulant may be carefully checked for physical properties such as viscosity and solids content at incoming materials quality control, and yet the final adhesion to the die and substrate may depend critically on some process control.

Photolithography and metal deposition and etching processes depend crucially on photoresist materials for circuitry and via formation in substrate manufacturing. Flux and solder pastes are important for volume assembly. Metrology for these materials is less important for their mechanical properties but is more important for parameters that impact manufacturing cost, product quality and yield. For example, high I/O fine pitch requires small solder pads. The variability of the quantity of solder paste on the pads provides a distribution of solder joint shapes which ultimately influences the joint fatigue life.

The impact of chloro-fluorocarbons, CFCs, on the environment and their pervasive use in the electronics industry in many processing steps from photolithography and solder assembly to other surface conditioning steps poses a severe challenge industry-wide. Environmental concerns on the potential risk of lead contamination may result in the curtailed use of lead-containing solder interconnections. Metrology research on the relevant properties would be the first important step in the search for alternate solvents and alternate interconnection systems.

ISSUES

Single chip packages have grown in complexity from relatively simple low I/O packages to high I/O fine pitch sophisticated packages. The capabilities of the materials and manufacturing processes are stretched to meet the new physical design and use environments. Many of the innovations in design and performance have been achieved as a result of advances in materials and processes, particularly in polymer materials. It is believed that better knowledge of the materials and intelligent design of the processes will contribute to future success.

Most polymer materials today are made by a small number of materials suppliers, many of whom are overseas. The materials properties information supplied is usually not extensive. Seldom is there information on the effect of processing or the properties when interfaced to other materials. The materials research community is seldom linked to the study of these materials, interfaces, and process sciences, nor is the materials research community usually linked to the mechanics community in relation to modelling, physics of failure, and the many phenomena of the materials encountered in manufacturing and field use.

Metrology represents the first step in understanding materials properties and their successful application in industry. It is also the basis for intelligent design of new materials and processes for future packages. A key issue is the knowledge of interfaces.

Interfaces between dissimilar materials are ubiquitous in electronic packaging. Indeed, not a small fraction of manufacturing processes are devoted to either tailoring suitable metallurgies or polymer surfaces to achieve interfacial strength or to clean those surfaces to remove undesirable contaminants. Examples are illustrated in the 10th figure of Barry Johnson's presentation (see Volume II, page 6, lower). In addition, the filled or reinforced polymer materials such as molding compound and laminate substrates contain inorganics (silica particles or glass cloth) which produce huge polymer/solid interfacial areas. These interfaces are potential sites for crack initiation and moisture residence. It is important to gain an understanding of these interfaces and how package failure mechanisms are related to the intrinsic nature of these materials.

The intrinsic properties of polymers do not necessarily change between bulk and thin film geometries. It is important to understand and account for interactions with adjacent materials in predicting the properties of thin films. For example, in thermal expansion, if a thin film is constrained in the plane of the film by a less expanding substrate, much of the normal volume expansion may be forced into the thickness direction and therefore the expansion may be much larger than the linear expansion reported for a bulk specimen. Similarly, the apparent moisture uptake of a thin polymer film on a substrate may be larger than a bulk sample if water accumulates preferentially at the interface. The interfacial region becomes more dominant as the film becomes thinner.

SUCCESS FACTORS

Principal demands on materials metrology for single chip packages are associated with measurement capability for specific properties in the configuration of use.

Reliable measurement tools for measuring material properties under conditions encountered in processing such as elevated temperature, pressure, and shear flow are important for providing quality products on time.

Comprehensive databases of material properties to enable design, manufacture, and assembly of electronic packages are strongly needed. Existing databases often list properties of bulk specimens which may be significantly different from material characteristics in the geometries of use. These databases are critical enablers for concurrent engineering of design, manufacture and reliability. They should document characteristics of commercial materials that reflect actual processing and manufacturing conditions such as elevated temperature, pressure, and shear flow for molding simulation.

Better understanding and techniques for surfaces and interfaces are required. Surfaces are ubiquitous to packaged products and measurements of silicon, copper, and various plated surfaces are needed to ensure process reproducibility and product reliability. A better fundamental understanding of adhesion is required. New and existing measurement techniques for characterizing interfaces like polyimide, epoxy, silicon, copper, solder, and variously plated surfaces under different conditions need to be applied to packaging structures where delamination and failure occur. Improved adhesion tests that relate results from stress testing to delamination encountered in practice are needed. Enhanced interfacial integrity can be achieved through improvements in adhesion and new materials which minimize stress at interfaces. Devising techniques to characterize the interfaces between several constituents in a package and relating those characteristics to the surface conditions during manufacturing is often the most important challenge.

MULTICHIP, HYBRID, FLAT PANEL DISPLAY

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INTRODUCTION

The scope of the working group on Multichip Modules, Hybrids, and Flat Panel Displays was to ...

> *... define and establish the critical issues facing the metrology infrastructure for the design, manufacture, and reliability assessment of materials and processes used in Multichip Modules, MCMs, Hybrids, and Flat Panel Displays, FPDs.*

To address all aspects of the packaging hierarchy appropriate to the working group, critical packaging and interconnect structures from *zeroth* up to the *second-level packaging*, e.g., from semiconductor chip to the electronic circuit assembly, were examined. In this commonly accepted hierarchy, the zeroth level consists of logic gates, transistors, and gate-to-gate interconnections. Discrete passive devices such as resistors and capacitors can also be loosely included. First-level packaging involves packaging of the chip or set of chips in a functional chip carrier. The latter can range from the simple dual in-line package, DIP, to complex thermal conduction modules with multiple individually cooled chips. The electrical connections are made through wirebonding, tape automated bonding, TAB, or flip-chip bonding.

Second-level packaging covers the assembly of the chip carriers onto a common base such as a printed circuit board or a ceramic substrate. The board may be composed of an organic material, a glass-filled polymer composite, a flex film, or an injection molded polymer. The substrate may be a multi-layer alumina or glass-ceramic based composite. All provide a medium for chip carrier-to-carrier interconnections, electrical testing, and off-board power and signal connections.

Although participation from the FPD industry was weak and no FPD champion led discussions on the subject, consensus exists that most of the technical issues related to the electronic driving portion of FPDs are sufficiently generic to be included within other discussions of the working group. For instance, chip-on-board, chip-on-glass, tape automated bonding, ball grid array, and small packages with thin profiles are some of the packaging needs required by FPD.

SUMMARY

Three major issues were addressed - insufficient material database; data relevancy and accuracy; and inadequate understanding of failure mechanisms - as they apply to multichip module, hybrid, and flat panel display packaging.

Industry-wide improvements in micro thermo-mechanical properties (<0.1 mm), interfacial properties, *in-situ* process monitoring, and high frequency (100 MHz-100 GHz) electrical properties are needed for meeting future product needs.

Development of environmentally conscious manufacturing techniques (e.g., lead-free solders), an unbiased assessment of scope, quality, and appropriateness for current materials databases, and the development of industry-compatible electronic data exchange formats require increased attention.

Large gaps exist in both disseminating information and linking related research and manufacturing infrastructure. Objective leadership in establishing standardized cost-effective test structures, test vehicles, and test methodologies for industry to use is especially needed.

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STATUS

Interfaces

All packaged components and systems are composite or multi-component structures with interfaces that can be potential sites for reliability problems. Interfacial delamination, cracking, or blistering are typical modes of failure commonly observed in a carrier. Better understanding of the interface properties will provide improved design rules, easier manufacturability, and products with enhanced reliability. The Working Group emphasized the importance of having good quality material data for design, modeling, and reliability prediction.

Databases

Existing databases for bulk material properties are presently of limited usefulness to industry for four major reasons:

Unlike inorganic materials, polymers have physical, chemical, thermal, mechanical, and electrical properties which are strongly process-dependent. Current materials databases do not cover a sufficiently wide range of processing conditions to allow extrapolation of properties under actual use conditions.

Packaging materials are mainly used in thin film forms under a variety of environments and constraints. The 'observed' properties of thin and bulk films often differ strongly. It may be argued that surface morphologies may differ in the two cases. The transition from surface to bulk properties is expected to occur within a distance of a few interatomic distances to perhaps tens of interatomic distances if surface morphologies are responsible for property differences. Furthermore, it may be argued that surfaces are more easily affected by their environment than the bulk. Thus, effects on the properties due to environmental moisture, chemical reactivity, or diffusion of foreign species can be expected to be more pronounced in thin films than in bulk materials. The transition distances from surface to bulk properties in those instances may be larger and exceed 1000 interatomic distances.

Constraints govern the behavior of the materials. Based on measurement of properties under simple constraints and thermodynamic considerations, predictions can be made about material properties under more complicated constraints. However, such a calculation can only be as good as the knowledge of the constraints, which may be unknown and difficult to assess.

The remaining challenge is the *in-situ* measurements of material properties. *In-situ* measurements of parameters determine what can be called "effective" or "apparent" materials properties. These measurements are generally conducted under complicated or assumed constraints and, by their nature, conceal the effects of constraints. Consequently, *in-situ* measurements may not give material properties which can then be transferred to varying situations and constraints.

ISSUES

The following summarizes and prioritizes the most important characteristics that were identified.

Cost-effective
This is the "litmus criterion" for wide industry acceptability. Test methods and standards have to be relatively simple for design and manufacture, and give unambiguous results on the failure mechanisms(s) observed.

Data relevancy and accuracy
Material properties for thin films or multilayer structures used in packaging are sketchy compared to bulk values. Basic properties are needed for developing elastic/plastic constitutive equations, hygrothermal behavior, microstructure property dependency, and interfacial properties. Effects of anisotropy need to be evaluated in greater detail. Even bulk properties are typically not available within the range of temperature, humidity, or constraint conditions that occur during actual use.

Bulk properties data for materials in constraint-free state are of basic importance and will continue to be needed. When used judiciously in conjunction with thin film properties measured under known constraints, intrinsic thin film effects can be decoupled from effects due to loading constraints or environmental factors.

Materials Databases
The present quality and coverage of databases for bulk properties of metals and ceramics is moderately good. However, information on polymers - especially in thin film form and under use conditions - is in dire need. Higher device performance and trends toward wireless applications demand more information on the high frequency (100 MHz-100 GHz) properties of packaging materials.

Another problem relates to the quality and appropriateness of available data and databases. Purdue's CINDAS database, for example, compiles materials data from numerous sources. These properties data often show wide variability due to the non-standardized test methodologies that are employed. This directly impacts the database quality. Also, relying on oft-simplified data supplied by vendors in product data sheets is no longer sufficient since property values will be process- and usage-dependent. Consequently, the appropriateness of data and conditions under which materials were processed must be considered for future database efforts.

Failure mechanisms
Current knowledge of failure mechanisms is rather limited. Delamination, corrosion, electromigration, film defects, dielectric breakdown are some typical examples of failures affecting the multilayer packaging structures. Anisotropy effects on thin films, for instance, can alter the failure mode of the packaged structure.

Product - process dependencies
The interrelationship between product manufacture and product performance is much more pronounced with polymers than with metals or ceramics. An understanding of these interrelationships is important for the design and manufacture of new products and processes. For example, the time-temperature cure program used in processing thermosetting polymers will affect the material's final properties. Such effects are not adequately considered and should be included in future databases.

Increased understanding
The influence of moisture, interactions with dissimilar materials, and the effects of environmental exposure require increased understanding. To fulfill this and the previously stated needs, increased development of test structures, *in-situ* measurements, and process monitoring is needed.

SUCCESS FACTORS

U.S. industry believes NIST can play an important role in leading the development of a metrology infrastructure for MCMs, Hybrids, and FPDs. This infrastructure needs to encompass test structures, test vehicles, reference materials, test methodologies, and failure models and needs to address fine-scale composite structures. The following technical issues dominate multichip module, hybrid, and flat panel display concerns.

- Metrology for micro thermo-mechanical properties (e.g., for features <0.1 mm), interfacial properties, *in-situ* process monitoring, and high frequency (e.g., 100 MHz-100 GHz) electrical properties
- Development of environmentally conscious manufacturing techniques (e.g., lead-free solders)
- Unbiased assessment of scope, quality, and appropriateness for current materials databases
- Industry-compatible electronic data exchange formats

Printed Wiring Board and Flex

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INTRODUCTION

Printed wiring boards, PWBs, and flexible PWB, or Flex, constitute a $25 billion market in which U.S. manufacturers have a diminishing part, currently, $5 billion of the total. Loss of this technology to off-shore suppliers is attributed to advantages of captive markets, i.e., the users of PWBs also make them, and to the disconnected and fragmented nature of the U.S. industry. Materials and equipment suppliers, electronic interconnection manufacturers, and OEMs constitute the PWB industry.

PWBs may be classified into three types based on their architecture and intended use. Characteristics of boards include overall dimensions, board and inner core thickness, number of layers, and line and hole sizes. The high performance boards, typically with 2-3 mil lines and 30-40 layers, find application in supercomputers and are a product class where U.S. industry dominates. Because of their limited use and the prominent U.S. technological position, there is little need for concerted industry/government action. The second type of PWBs typically employ 3-4 mil line widths and 4-16 layers. The trend here is for lighter weight, thinner layers, and flexibility to accommodate higher line and via densities, or to accommodate smaller and tailored formats such as required by chip carriers. These products were viewed by the working group to be an important segment for U.S. to regain market share. The third type contains 1-6 layers and >6 mil lines and is found in mass-produced consumer products largely manufactured off-shore by companies that make the PWBs themselves. An exception is the U.S. automobile industry with their large U.S. manufacturing base. For this reason other U. S. firms feel that they cannot compete favorably in this product line.

Flexible PWB are used in applications where planar structures cannot be used. They usually are polyimide- or polyester-based, rather than epoxy, and are generally not reinforced. The current market for flexible boards is much smaller than for rigid boards but is growing especially for telecommunication applications. Consumer electronic products that are manufactured off-shore often use flexible boards.

Discussions of the Printed Wiring Board and Flex Working Group included:

- enumeration of the challenges facing this industry;
- technological advancements that determine future market needs;
- priorities in materials metrology, knowledge base and data.

SUMMARY

Metrology and data issues within six major themes were identified and believed important to the future health of the U.S. PWB and Flex industry.

Materials
Improvements in materials properties are believed needed, possibly through introduction of new materials. Most important among them include: higher Tg; lower dielectric constant; smoother surfaces; and CTE match to copper. New materials development should strive to utilize existing manufacturing infrastructure to minimize the cost of their introduction.

Design
Improvements in design should strive to: lower manufacturing costs; create design tools for direct-chip-attach and reduced time-to-market; minimize effects of moisture on PWB performance; improve interfacial adhesion; enhance dimensional stability; and develop data for plated through-hole, PTH, copper.

Manufacture
Manufacturing must reduce its costs without adversely affecting performance. Manufacturing showstoppers for PWB fabrication include: laminate and foil finish; testing efficiency; number of process steps; vertical partnerships; process availability and control; and environmentally friendly processes.

Technology is needed to manufacture PWBs and Flex consisting of very thin (2 mils or less) layers, fine lines, small vias, and patternable vertical interconnections. Test methods need to reflect actual conditions in the manufacturing process. Advances in measurement methods to assess performance of finished products during manufacture will reduce rejection rates.

Reliability
Highest concerns in reliability and performance of PWB's and Flex are linked to improved interfaces, better moisture control and higher dimensional stability. Accelerated test methods that measure true failure modes are needed. New substrate materials with higher operating temperatures, lower coefficients of thermal expansion and lower moisture sensitivity is viewed as one approach to addressing these issues.

Modeling and Simulation
Shortened time-to-market goals necessitate development of integrated software packages that perform CAD functions and simulate thermal, electrical and reliability performances using appropriate materials databases. Software packages that directly relate designs, based on chip sets input, to manufacturing data bases in the factory are equally important. Models linking the variation in mechanical properties with manufacturing processes are needed for refining processing conditions, i.e., temperature and pressure, and optimizing properties through processing.

Technology Environment
New comprehensive strategies are needed in technology development, data usage, and manufacturing to achieve competitive advantages in response to these technology drivers. This also includes the organizational structures needed to attain those advances. Reliance on large U.S. companies to lead technology development is believed outmoded within the present industrial framework and responsibility for research and development will likely shift to new entities. However, it may be difficult to develop technology within consortia because of the anticipated slow pace of progress.

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STATUS

Four primary market drivers exist for PWBs and electronic equipment.
- lower costs
- greater miniaturization
- enhanced performance and reliability
- rapid innovation of products to keep pace with chip-level advances

Most member companies of the IPC manufacture multilayer boards and serve customers whose primary driver is time-to-market. To be efficient these suppliers must operate on very low overhead which limits their ability to invest in the research and development that stimulate technological advances. In this environment the source of new technology developments is a concern. In the past, innovation took place in large corporations such as IBM.

The working group observed that little is known in this business about materials metrology, effects and differences due to size, and the statistical significance of measurements being made by industry with respect to PWB and Flex materials. The all-too-frequent approach when materials problems arise is for the industry to produce short term fixes by designing around them. This approach does not improve fundamental understanding and fails to meet future needs in existing and new products. To a great extent industry relies on age-old tests that may no longer be relevant and may not relate to field performance. With the advancements in MCM-L, SCM-L, and chip-on-board attach, PWB manufacturers have a great opportunity to provide customers with low-cost solutions for high I/O chip carrier needs.

CRITICAL MATERIALS, STRUCTURES & PROCESSES

The principal materials constituting PWBs and Flex are organic insulators, generally glass-reinforced epoxies, and copper conductors. PWBs are layered structures of epoxy insulators, layer thicknesses of 4-6 mils, with patterned copper conductors and copper plated through-holes (vias) connecting the various layers. Good adhesion between conductor and insulator, and between neighboring insulator layers is crucial to performance and reliability. High dimensional stability is required to maintain electrical connections; thermal cycling during manufacturing and the large difference in CTE between insulator and conductor tend to lead to dimensional instability.

The statistical significance of measurement data, such as physical and mechanical properties, derived from either existing or new methods, was debated by industry members of the working group. A knowledge base of statistically significant sample size on realistic specimens (with *in-situ* dimensions, such as in thin films and passivation layers) is needed as a precursor to introducing the new measurement methods into practice. Similarly, in order to apply models to real applications, the models should be calibrated against measurement methods and data and then extended through further correlations and extrapolations.

Insulators

The problems of dimensional stability, interfaces and moisture retention may be mitigated by different choices of substrate materials. Fluorocarbon polymers are viewed as more desirable in terms of dielectric properties, thermal stability and CTE than existing epoxies. The processing science for these potential replacement materials has not been established, however. Thermoplastic liquid crystalline polymers are another potential replacement material which have the advantage of tailored CTE by preferential alignment of the polymer molecules.

Conductors

Lack of characterization and measurement methods for thin foils, fine circuitry, and via structures is a concern. One key process in manufacture is electroplating of copper in cylindrical geometries. Properties of copper in PTHs, in particular kinetics and mechanical properties (stress/strain), and relationships between properties and failures are poorly understood. Better measurements of thickness of copper in vias are needed to test predictive models of deposition and performance.

Manufacturing Processes

The focus on lower manufacturing costs extends to lamination, circuit patterning, drilling, via formation, and parallel or sequential layer fabrication. Currently, research is lacking on alternate techniques to form holes. Mechanical drilling may be replaced by laser drilling or chemical procedures such as photolithography of photosensitive dielectrics. Integration of CAD software to include predictions of thermal, electrical and materials performance would facilitate introduction of new materials. Processing models would extend to predictions of variations in the mechanical properties and dimensional response of materials to processing variables. A requirement of such software is the availability of data compatible with design tools. Environmental concerns with existing processes were expressed and it was concluded that new processes should be environmentally benign.

ISSUES

Improved Dimensional Stability

Lower costs can be achieved by manufacturing large panels, but dimensional instability is a problem because through-holes may not be properly aligned. In addition, trends towards thinner cores will produce less stable structures. Prediction of dimensional response to processing needs improvement. As long as dimensional changes can be predicted, then they may be accommodated for in mask generation and manufacturing.

While macroscopic models based on the viscoelasticity of the resins may be useful, consideration of the microscopic structure, e.g., the presence of dissimilar materials and voids is likely important. Etching away large amounts of copper in large sheets creates large excursions in dimensions. The issue of dimensional stability relates to the microscale behavior where better understanding is needed to provide better microscopic models (voids, and void coalescence, elastic-plastic behavior, solder joints) and relationship to macroscopic behavior. Better microscopic models would improve materials behavior prediction with regard to:

- viscoelasticity effects
- Poisson's ratio
- modulus
- yield values
- tensile properties

Insulator Materials

Insulator materials include fluorinated polymers, such as PTFE, liquid crystalline polymers and fiber-reinforced (FR) class of epoxy resins. Epoxies will continue to be used because of their low cost. Lower dielectric constant substrates for high frequency requirements drive the use of fluorinated polymers. Liquid crystal resins are another class of likely candidates for substrate materials, particularly in thin structures because of the ability to tailor the CTE in three-dimensions. Non-woven polyaramid fiber reinforcements are emerging for DCA applications. Photosensitive dielectrics based upon solder mask technology are new exciting developments.

In the manufacturing and use environments, moisture and its effects on PWB quality and performance are key issues. It was pointed out that at least six different methods of measuring total moisture exist, none of which agree. Of more relevance, however, is the location, or distribution of the moisture and not merely the total content. What are permitted moisture levels relative to materials properties and cure characteristics? Data on volume changes associated with moisture adsorption are needed as is knowledge of degradation mechanisms and accelerated test methods. Differences in opinion exist regarding how dielectric properties are influenced by moisture. Models are needed that include the role of manufacturing defects on the kinetics of moisture uptake, its distribution and equilibrium values.

Interface Phenomena

Perhaps the most striking feature of PWBs and Flex is the prominence of interfaces. Interfaces between silicon and insulator, insulator and conductor, and between insulators are subjected to various thermal environments during manufacture. The prevalence of interfaces leads to critical concerns in adhesion and delamination due to CTE mismatches. Interface delamination and a poor understanding of Cu-thermoset and thermoset-glass interfaces are big problems. Adhesion is also important in die attachment. A need exists to relate interphase adhesion to delamination and stress parameters. The lack of data and knowledge bases, particularly regarding adhesion and its durability, limit application of time-to-market strategies.

Suitable test methods for adhesion do not exist. Lap shear and peel tests, the currently favored industrial methods, are appropriate for quality control, but not applicable or reliable for quantitative models. It is generally observed that no correlation exists between the results from these test methods and the performance of structures and that the methods do not properly rank material performance. Better measurement methods that are available in university, government, and industry research laboratories need to be brought into widespread industrial use.

Improved adhesion of polymer to copper is not articulated in the IPC Technology Roadmap. Presently copper is chemically or mechanically treated to improve adhesion to the dielectric. This treatment, however, can result in poorer electrical signal propagation characteristics. Procedures are needed to chemically bond polymers to smooth copper surfaces. Currently, Cu is roughened to increase surface area.

Trends to higher frequencies will drive the technology to alternate substrate materials such as fluorinated polymers and poly(tetrafluoroethylene). A challenge is to improve bonding of fluorinated polymers to metallized surfaces and to each other.

Computational methods for predicting interfacial adhesion would be highly desirable. The computational models should include assessment of coupling agents and their effectiveness with regard to glass and metal surfaces. Extending computational methods to real structures would permit treatment of durability and environmental factors affecting interfaces as well as the criticality of debonding.

Electrical Characterization
In addition to the materials metrology needs enumerated above, the issue of how electrical measurements were made was discussed. Measurement of impedance (all frequencies are included) leads to different conclusions than capacitance measurements (which are performed at specific frequencies). Currently, impedance measurements are performed on boards. Although more sophisticated techniques are available in research laboratories, their use by manufacturers is limited by cost, level of technical expertise, and adaptation to manufacturing environment.

SUCCESS FACTORS

Materials
Improvements in the following materials properties are believed needed. These improvements may arise through introduction of new materials.

- Higher T_g for higher operating temperatures
- Lower dielectric constant for faster signal times
- Smoother surfaces for capability of fine lines with adequate adhesion
- Match of CTE to copper to improve reliability

Adhesives are widely used for bonding in flexible boards. Advances in materials and processes aimed at eliminating adhesives were viewed desirable for these applications. New materials development should strive to utilize existing manufacturing infrastructure to minimize the cost of their introduction.

Design
Improvements in design should strive to achieve the following:

- Lower manufacturing costs
- Create design tools for direct-chip-attach and reduced time-to-market
- Minimize effects of moisture on PWB performance
- Improve interfacial adhesion
- Enhance dimensional stability
- Develop data for plated through-hole, PTH, copper

Manufacture
The key goal in manufacturing is to reduce cost without adversely affecting performance. For high performance boards this may involve entirely new fabrication approaches. Manufacturing issues among the IPC list of showstoppers for PWB fabrication include:

- Laminate and foil finish
- Testing efficiency
- Number of process steps
- Vertical partnerships
- Process availability and control
- Environmentally friendly processes

Technology is needed to manufacture PWBs and Flex with new core materials that can be processed in layer thicknesses of less than 2 mils and with reduced hole formation costs. Similarly, technology is important for patterning fine lines and vertical interconnections to take advantage of thin layers and small vias. Advances in measurement methods to assess performance of finished products in the course of manufacture would improve rejection rates. Test methods, in general, should be more reflective of actual conditions in the manufacturing process.

Reliability

Highest concerns in reliability and performance of PWBs and Flex are linked to improved interfaces, better moisture control and higher dimensional stability. Accelerated test methods that measure true failure modes are needed. New substrate materials with higher operating temperatures, lower coefficients of thermal expansion and lower moisture sensitivity are viewed as one approach to addressing these issues.

An identified problem concerns the stability of through-hole vias. One major limitation of flex is that the thermal expansion coefficients of constituent materials in vias vary widely which can precipitate failure through thermal cycling.

Modeling and Simulation

Shorter times-to-market necessitate the development of integrated software packages that not only perform CAD functions, e.g., route wires, but also to simulate thermal, electrical and reliability performances using appropriate materials databases. Equally important are software packages that directly relate designs, based on chip sets input, to manufacturing data bases in the factory, thereby skipping intermediate steps and speeding time-to-market.

Models linking the variation in mechanical properties with manufacturing processes are needed for refining processing conditions, i.e., temperature and pressure, as well as optimizing properties through processing. An example is a prediction of the dimensional response of materials to processing which would allow better control of the dimensions of the finished product.

Technology Environment

To achieve competitive advantages in response to these drivers, strategies must focus on changing the way we develop new technologies, use data, and manufacture products. Equally important to what technological advances are needed is the organizational structure to attain those advances. Reliance on large U.S. companies to lead technology development is outmoded given the present composition of the worldwide industry.

Individual companies often focus on short-term solutions rather than research and development to sustain progress. Responsibility for research and development will likely shift to new entities. Time constraints may make it difficult to develop technology under consortia because of the anticipated slow pace of progress. Differences existed among working group participants on the types of PWB products that should be highlighted in future NIST/Industry efforts.

Electrical and Optical Interconnection and Assembly

Greg Munie, AT&T Bell Laboratories
Carol Handwerker, NIST Metallurgy

INTRODUCTION

The scope of the group was defined by the attendees to be all aspects of electrical and optical interconnections from design through component choice, assembly, and test. Electrical and optical interconnections are the critical links between individual chips, components, devices and functioning systems. The materials, structures, and processes used in forming electrical and optical interconnections are influenced by the performance needs and characteristics of the individual components that are being linked.

SUMMARY

Critical deficiencies exist in the materials metrology and data that is available for the design, manufacture, assembly and reliability of both electrical and optical interconnections. Derived from these deficiencies, priorities for improved test design, model development and property measurement were established. These include:

Design/Manufacturing

- A predictive test of manufacturing solderability for in-line process control
- Tolerances and measurement techniques for component placement errors
- Tolerances and measurements of component lead co-planarity
- Measurements of intrinsic alignment stability of optical interconnections
- Measurement of feature accuracy intrinsic to lithographic patterning
- Measurements of optical properties and development of databases

Reliability

- Validated accelerated mechanical and thermal reliability tests and models
- In-line process control and inspection for interconnection reliability
- Factors influencing interconnect mechanical properties and reliability
- Laser reliability
- Accelerated diagnostics assessing transmission accuracy of optical systems

The lack of integrated modeling tools for design, manufacturing, and reliability assessment of interconnections is viewed as a major problem in the electronics industry and was identified as a "show stopper" in the 1993 Semiconductor Industry Association (SIA) Technology Roadmap.

Leadership
The working group believes leadership is needed in bringing together industry representatives to create an environment conducive for open exchange of non-proprietary data and information among companies, and identify means and methods for addressing industry stated needs.

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STATUS

Poor cooperation generally exists between the designer and those responsible for the manufacturing, assembly, and reliability assessment of interconnection systems. A designer typically uses simple formulas to choose materials and structures for a design based on performance and cost. The assembler then tries to find an acceptable way to form interconnections using the materials/processes chosen by the designer. The reliability assessors are then given the final product to determine whether it passes some tests that correlate with performance in the field. The process of converting a design to practice is largely empirical and frequently lacks coordination or cooperation from the designer, to the assembler and to the reliability engineer, with little iteration or information passed.

CRITICAL MATERIALS, STRUCTURES, PROCESSES

Table II illustrates the variety of materials, structures, and processes used in forming electrical and optical interconnections that were viewed critical to today and tomorrow's electronics industry. In addition, other materials, structures, and processes associated with microelectronics impact interconnection metrology and data. These include Known Good Die (KGD), silicon technology, substrates (MCM-L,-D,-C, flex, rigid), detectors and other components, chip on glass packaging, lead frame/design, and die attachment.

Table II: Critical Electrical and Optical Interconnection Materials, Structures, and Processes

Materials:	**Processes:**
copper	machining (laser/mechanical/etc.)
aluminum	soldering (all levels: chip and above)
leaded and lead-free solders	plating
electro-optic polymers	cleaning
conductive epoxies	overcoating/sealing (hermetic sealing)
	fiber preparation (cleaving, etc.)
Structures:	laser to fiber alignment (single and
cables	multimode; formed by solder)
strip lines	thin film deposition
connectors	rework
wire bonds	microlithography/microfabrication
direct chip interconnection	dielectric polymer deposition
thin film metallization	robotic assembly
package feed-throughs	final assembly
vias	optical calibration
lasers	reliability assessment
fibers	systems testing
waveguides	
lenses	

At the systems level, the characteristics by which electrical and optical interconnections are evaluated are design and performance, reliability, and cost. These metrics are interrelated, but present design tools and data that allow them to be balanced against each other are limited or non-existent. Furthermore, existing performance and reliability models are based on the behavior of bulk materials and may not be applicable at the small size scales and in the geometries present in electronic and optical interconnections.

ISSUES

The lack of realism in available materials data for interconnections is a major obstacle to improving performance and reliability and lowering cost. Furthermore, the available data is generally for bulk materials and consequently may not reflect real world use, design needs, or assembly processes in microelectronics and integrated photonics.

An allied issue is the existing gap in test philosophy and methodology for providing data and modeling for relevant structures and processes. The poor cooperation and coordination that typifies present interconnection development needs to be replaced with a "right data, first time, within cost" approach for test design. The key features of this test philosophy and methodology as applied to electrical and optical interconnection are:

- Establish realistic standard test conditions applicable to available component and interconnection structures.
- Design realistic test specimens so that useful data can be obtained in a timely and cost-effective fashion.
- Develop cost-effective validated models relating test results to interconnection design, manufacturing, and reliability. These models must be able to assess the impact of materials property variability since statistical failure distributions are expected in all processes. The effect of materials variability in packaging is not well understood.
- Produce reference materials for standard structures.
- Establish an iterative system for updating tests, materials, structures, and methodologies.
- Provide an industry - national laboratory forum where companies can assist in test design and implementation, share data without compromising company confidentiality, and have access to materials databases.

SUCCESS FACTORS

Critical priorities for metrology, data and modeling covering design, assembly, and reliability were identified. These success factors are applicable to all types of interconnections, for example fine pitch, BGAs, and optical components.

Leadership is needed to bring industry representatives together and create an environment that encourages the open exchange of non-proprietary data and information among companies, and creates a means and method for addressing industry stated needs. As one industry participant stated, "...industry needs an interest group that focuses on users and concurrent systems issues. Design, manufacturing and assembly, and reliability must be [well coordinated] all related - and no 'throws-over-the-wall' should be possible or allowed." It was suggested NIST could be the catalyst for creating this environment.

A key success factor for interconnection and assembly is the integration of all three stages of the product development cycle - design, manufacturing, and reliability - using expert modeling tools. Such tools are required to make the best choices among the various interconnection materials, structures, and processes listed in Table II in relation to cost, performance, manufacturability, and reliability.

The following factors were identified to constitute the highest priority needs in relation to materials metrology and data for electrical and optical interconnection. The working group strongly endorses the methodology described above that reflects the "right data, first time, within cost" approach for all of the following.

For Design and Manufacture

A predictive test for manufacturing solderability for in-line process control
Considerable resources are now used to improve component and board solderability immediately before assembly and to repair or rework solder joints on assembled boards. A reliable test for predicting manufacturing solderability would allow the design of in-line process controls at earlier processing stages for boards and components.

Tolerances and measurement techniques for component placement errors
When components are placed on boards away from their optimum positions, some amount of repositioning can take place during solder reflow. If the initial placement error is large, the repositioning during solder flow may not be sufficient for proper component alignment. It is, therefore, important to know the intrinsic accuracy of component placement processes.

Tolerances and measurements of component lead coplanarity
Lack of coplanarity in the leads and other deviations from design geometry affect the solder wetting of leads, the alignment of optical components, and the thermo-mechanical response of components during use. The definition of acceptable limits depend on the geometries of components and boards and the type of interconnection employed.

Measurements of intrinsic alignment stability of optical interconnections
Reproducible alignment of optical interconnects is necessary for optical systems to gain widespread acceptance in microelectronics. An understanding of the tolerance limits for optical fibers and components and the errors inherent in alignment processes for optical systems is critical to lowering insertion loss, i.e., improving reproducibility. Tests for examining the stability limits of alignment processes, including soldering, laser welding, and adhesive attachment are needed. Additional tests are needed to assess the loss of alignment during use due to creep and fatigue of the attachment material. Mechanical properties data is needed for optical attachment materials.

Measurement of feature accuracy intrinsic to lithographic patterning
Optical devices and interconnects are frequently manufactured using lithographic processes and device performance often varies substantially over the large areas being processed. This variability is dependent on the starting materials, including photo-resists, and on the lithographic processing steps. Understanding the relationship between the lithographic processing of materials, the structures formed, and their resulting properties are needed.

Measurements of optical properties and development of databases
Data on the variability of linear and nonlinear optical properties with composition, processing, and other parameters are important for predicting the performance of optical interconnect systems.

For Interconnection Reliability

Validated accelerated mechanical and thermal reliability tests and models
The reliability of electrical and optical interconnections depends on the thermo-mechanical fatigue behavior and vibration/impact response of an interconnect system. Validated models of reliability and accelerated mechanical and thermal reliability tests are needed to improve interconnect design.

In-line process control and inspection for interconnection reliability
In-line inspection methods and process controls are needed for the real-time identification of features associated with known failure modes in interconnect systems.

Factors influencing interconnect mechanical properties and reliability
Mechanical property measurements must be obtained as a function of time, temperature, processing, and component geometry in order to assess mechanical reliability. Reliability modeling can be used to help identify which data are needed.

Laser reliability
Standard tests are needed to assess the lifetime, wavelength accuracy, and power of laser sources used in optical interconnection.

Accelerated diagnostics for assessing transmission accuracy in optical systems
With the enormous increase in speed of data transmission offered by optical systems, new ways of testing the accuracy of the transmitted data are needed. Two specific needs identified by the group are diagnostics for analyzing bit rate errors, and a high speed optical parallel channel data link test for laser arrays. These diagnostics should cover both system errors and should be able to identify failing subsystems.

TECHNOLOGY SUPPORT

ELECTRICAL

Eric Bogatin, Sun Microsystems
Roger Marks, NIST Electromagnetic Fields

INTRODUCTION

Regardless of package, integrated circuits need to be electrically interconnected. A primary requirement of packaging is to provide those interconnections. The electrical performance of the package, as described by parameters such as bandwidth, impedance, propagation delay, loss, and crosstalk, delineates the system performance. Lacking definitive means of assessing these parameters, industry may either under-design the package, at the risk of system failure, or over-design, at the expense of unnecessary cost. Either scenario can doom the product.

Electrical design cannot be approached without proper measurement tools. While metrology does not lead directly to design, it does contribute to design tools by providing good data on materials and material structures for use in simulation and by validating, or indeed *in*validating, simulation tools.

The scope of the working group on electrical properties included electrical measurements for packaging and interconnection of microelectronic systems, focussing particularly on the methodologies and test structures needed for characterizing materials, processes, and structures at high frequencies (over 10 MHz), where problems typically occur. The preliminary reports of the technology-focused working groups were examined and concerns related to electrical metrology and data were aggregated. These concerns emphasized the following requirements:

- measurement philosophy and methodology
- *in situ* measurements
- standard test procedures
- standard test structures and reference materials
- disparity between user and supplier methodologies
- technology diffusion from the research environment

Based on these concerns, discussions were not limited to measurements of bulk material properties, but also included electrical characterization of structures. The determination of intrinsic material properties is necessary for developing fundamental understanding but is insufficient for purposes of product design, manufacture, and reliability assessment. Material properties are often process-dependent and are sensitive to interfaces and surface features in thin-film formats. Even with exact materials electrical data, electromagnetic field simulation tools may still fail to predict important electrical effects that may be measurable and significant due to approximations such as ignoring conductor loss or surface roughness. Consequently, fabricated material structures may be difficult to understand based solely on material properties and a broader approach, including structure measurements, is required.

SUMMARY

Demands for improved electrical performance of semiconductor components and assembled systems are driving developments in high performance packaging. However, the actual performance of any packaging system is difficult or impossible to ascertain without careful electrical measurements. Such measurements can provide the data needed to make rational choices as to which technology can provide the required performance and reliability at the lowest cost. These electrical data support materials characterization, system design, process development, process monitoring, and product specification. Overall industry awareness concerning proper electrical characterization methods and analysis is limited and industry-wide standard testing methods are badly needed. Specific recommendations include the following.

- Exploit existing on-wafer microwave metrology
- Develop and promote time domain techniques
- Develop standard testing methods and structures
- Establish a certification process for independent laboratories
- Promote improved education and training

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STATUS

Industry awareness of the importance of electrical issues is reflected in the growing involvement in standards activities such as the JEDEC JC-15 Committee on Electrical and Thermal Characterization of Semiconductor Packages and Interconnects. While companies demand new standards, many issues require additional study which often exceeds committee resources. Industry's limitations in conducting measurements are *not* due to the unavailability of appropriate instruments but instead to other factors:

Insufficient understanding, training, and expertise
Industry's ability to measure accurately electrical characteristics of packaging and interconnect structures is insufficient to satisfy emerging needs. Historically, the packaging industry has not allocated sufficient resources to electrical problems. Companies will continue to face difficult challenges in finding specialists with appropriate electrical engineering and measurement expertise.

Lack of industry consensus
Lack of industry consensus concerning methodology, test structures, measurement conditions, and interpretation seriously hampers the utility and value of electrical measurements. Companies lack confidence in their own data as well as that of their competitors and suppliers.

User-unfriendly methods
Methods that are viewed to be accurate are also viewed as unwieldy, complicated, expensive, and time-consuming and therefore suitable only for use in research laboratories.

Failure to apply appropriate calibration techniques
Critical electrical measurements typically utilize high-performance instruments such as network analyzers and time domain reflectometers. Unfortunately, their performance is limited by their calibration, particular for measurements on devices and package substructures. Network analyzers are normally used with extensive calibration but conventional methods can be inappropriate for many packaging and interconnect measurements. In the case of time domain reflectometers, thorough calibration is rarely performed.

Intrinsic *versus* extrinsic measurements and characteristics
Confusion widely exists as to the distinction between *intrinsic* properties, which pertain to bulk materials, and *extrinsic* characteristics, which describe material structures. For example, printed wiring board, PWB, suppliers frequently specify the dielectric constant or permittivity of the bare board. However, the *effective permittivity*, which can be determined by transmission line measurements, is a property of the transmission line structure and not of the bare board alone. While both measurements are important, it is the transmission line measurements that provide the bottom-line electrical performance parameters for an assembled PWB, including propagation velocity, loss, and characteristic impedance. These depend on the permittivity of the dielectric and on associated factors such as the metal conductors, geometry, and configuration.

ISSUES

The working group identified a number of critical issues and gaps that impede the assessment of electrical performance in advanced packaging and interconnections:

Standard test procedures, reference materials, and structures
The lack of standard test procedures diminishes confidence in measurements and thereby diminishes the value of measured data. Significant improvements can be gained from proper calibration and measurement procedures using available

instruments. Many test procedures cannot be standardized without the use of standard test structures and/or reference materials for calibration and verification. The present disparity in measurements, conducted by users and suppliers, could be eliminated through the efforts of standards committees.

***In-situ* measurements**
The importance of *in-situ* measurements in manufacturing environments was repeatedly stressed. This demands the characterization of specific structures as found in actual devices and that measurement methods be sufficiently robust to find use in manufacturing environments and not solely in the research laboratory. The resulting data, in conjunction with electrical property measurements of bulk materials, may be useful in developing a fundamental understanding of the specific factors that cause the characteristics of the structure to differ from the pure material.

Technology diffusion from research labs
Many technological innovations required to address the problems in electrical measurement are believed to exist within government and industry laboratories. However, industry has not been able to make use of this knowledge. The technical knowledge that resides in these centers of competency must be applied to prevent wasteful allocation of future resources.

SUCCESS FACTORS

Broad-based adoption of standard calibrated techniques
Conventional network analyzer calibration techniques are unsuitable for on-wafer and many packaging and interconnect measurements. Improved methods, developed by industry and government laboratories, are available. Suppliers and users alike must adopt these techniques to ensure accurate and meaningful results and to ensure the exchange of high quality data.

Calibrated time domain techniques
For many purposes, time domain measurements have the capability to provide needed data at low cost using fast, simple techniques and instrumentation. Presently, however, time domain systems are used with little or no calibration or error correction. Accurate calibration and de-embedding techniques and methodology are needed. Many have already been developed but are not widely utilized. The successful application of time domain instruments requires that calibration and measurement methods be fully validated and standardized.

Physical standards
Physical standards are required for electrical measurements. In many cases, the fabrication facility may need to produce calibration standards at the time test devices are fabricated. In this case, the facility needs to be aware of the requirement and have access to design procedures for standards. In other cases, particularly when commerce is at issue, global standard reference materials may be necessary. Permittivity measurements may require characterized bulk materials for calibration or verification of measurement systems.

Test fixtures and structures for simulating in-process and in-use measurements
In-process and in-use measurements demand specific test environments. Factors such as frequency, temperature, humidity, and mechanical stress can significantly influence electrical behavior. This places strict demands on controlled testing under diverse environments.

Better modeling tools
The computation of "extrinsic" structure parameters from a knowledge of "intrinsic" material properties requires a detailed understanding of the product-process relationships and of factors such as boundary conditions. Existing modeling tools often fail to account adequately for important electrical effects. Accurate measurements allow the validation of design tools and stimulate their refinement.

Education
Manufacturers, suppliers, and users all need to be aware of electrical issues and available measurement methods.

RECOMMENDATIONS

Exploit existing on-wafer microwave metrology
The digital packaging industry has not concentrated on electrical characterization to the extent found within the microwave industry. Existing microwave metrology has direct application to high performance packaging and interconnection measurements, particularly in the measurement of scattering parameters using on-wafer probes and calibration with standard test structures. The availability of accurate microwave measurements has enabled the introduction of design libraries composed of measured data on elementary structures. This notion should be applied to advanced package designs.

Develop and promote time domain techniques
Traditionally, the most reliable electrical measurements have been performed using frequency domain instruments, including automatic network analyzers. However, the capital expense and expertise required to support a network analyzer may be prohibitive. Time domain techniques, including fast digital oscilloscopes, are low in cost and readily available inside most laboratories. These techniques should be more fully developed, standardized, and disseminated throughout industry.

Develop standard testing methods and structures
Standard-setting requires a partnership among NIST, industry, and standard-settings organizations. Industry generally prefers not to expend significant resources to develop, characterize, or document metrology. Industry believes NIST should work to develop the needed metrology and work closely with standard-setting bodies such as ASTM and JEDEC JC-15. A lack of industry commitment to participate in such organizations may sharply limit this process.

Establish a certification process for independent laboratories
Independent laboratories with capabilities for conducting precision high frequency measurements should be accredited to insure reliability and accuracy of test results. NIST should apply its National Voluntary Laboratory Accreditation Program, NVLAP, in this area of high frequency electrical measurements.

Promote improved education and training
Industry in general is confused about the roles of the various government agencies and industry groups. A broadly adopted forum is needed to educate and train industry about government resources as well as existing and newly-developed methods. NIST, universities, consultants, professional societies, or trade groups may be appropriate members of such a forum.

OPTICAL

Davis Hartman, Motorola
Joseph A. Carpenter, Jr., NIST Ceramics

INTRODUCTION

The scope of the working group on optical properties was determined by first identifying the most important design considerations for optical systems; these are given in Table III. Then, the most important design considerations for the modules comprising those systems were identified. These are given in Table IV. Finally, the most important structures of those modules were identified; these are identified in the text below. The scope was therefore to identify gaps in the metrology and/or data pertinent to those structures.

Table III: Design Considerations for Optical Systems

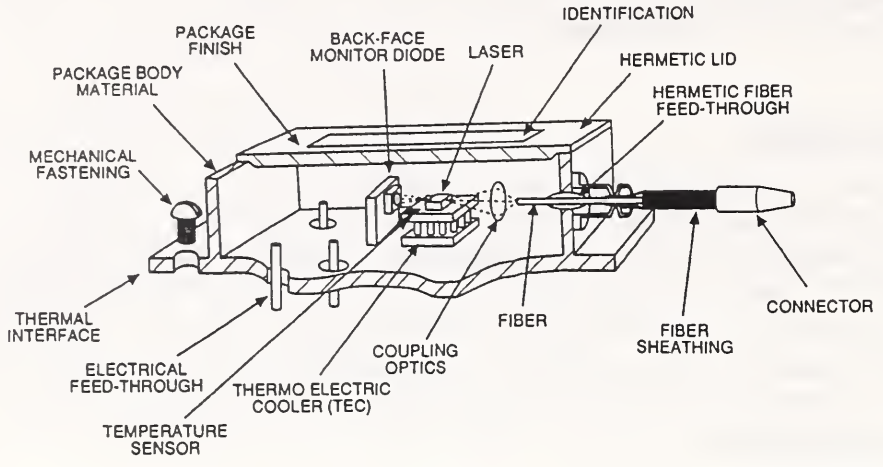
Cost	Power Consumption
Reliability	Size & Weight
Speed/Bandwidth	Ergonomic
Crosstalk (Bit Error Rate)	Radiation Hardness
Data Handling (Coded, Burst, etc.)	Hermeticity
Operating Temperature	Military vs. Commercial Specifications
Storage Temperature	Length
Environmental	

Table IV: Design Considerations for Optical Modules

Temperature Drop	Encapsulation Strategy
Thermal Resistance	Power Distribution
Optical Power Budget	Clock Distribution
Lead Frame Design	Vias (Thermal)
Vias (Electrical)	Mother Board
I/O Definition (Logic Levels, Differential vs. Single-Ended Coupling)	Form of Optical I/O (e.g., pig-tail, connector, or waveguide)

Figure 1 illustrates a typical optical module and the structures that comprise it. In this example, the back-face monitor diode, laser, coupling optics, fiber, fiber feed-through, fiber sheathing and connector are the optical or optic-related structures. The other structures illustrated are typically found in electronic components and were not addressed by this group.

Figure 1: Major features of a typical state-of-the-art laser module [9].



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SUMMARY

Success factors were identified that apply to: optical waveguides; sources and detectors; modulators, wavelength multiplexers, selectors, and isolators; micro-optics and coatings; connectors and optical alignment; substrates; die attachment; and die encapsulants. Within the scope of these success factors, five primary cross-cutting metrology and/or data issues were viewed as important to the future implementation of optical assemblies and interconnects. They include:

- Metrology for and data on thin-films, especially of polymers
- Dimensional metrology, especially for nanostructures
- Characterization of surfaces and interfaces
- Expanded properties databases
- Non-contact, spatially resolved temperature measurement

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STATUS AND ISSUES

Databases
The working group concluded that the perception that arose in the technology-focused groups that databases containing optical properties of packaging materials currently don't exist, is substantially, but not totally, correct. There are a few publicly or semi-publicly available databases on packaging materials, but the optical properties are often added more as afterthoughts and there are large gaps in the coverage.

Optical Waveguides
Optical waveguides are structures that transmit light through internal reflection and are surrounded by another medium of lower refractive index. Optical fibers and channel- and planar-waveguides are common examples. The term is often used to describe a passive device in which the waveguide is neither optically nor electrically active. In other words, its only function is to transmit light. Important considerations include:

- optical loss due to absorption and scattering by the waveguide material (referred to as "material loss");
- optical loss due to light leaking out of the waveguide (referred to as "waveguide loss"); and
- temperature.

Dispersion due to the variation of refractive index with optical frequency is not a significant problem except in long-distance fiber-optic systems.

Sources and Detectors
Sources provide optical illumination. Light emitting diodes, LEDs, and laser diodes, LDs, are the prevalent types. The optical signal can be shaped either by modulating the electrical power to the LED or LD or by externally modulating the light.

Detectors convert optical signals to electrical signals. Almost all the optical detectors used in modern optical systems are photodiodes, mostly single p-type semiconductor - insulator - n-type semiconductor, PiN,; avalanche photodiode, APD,; and varieties and arrays thereof. A major area of concern for detectors is failure mode analysis. Questions arise as to whether the same mechanisms that cause failure in detectors operating near room temperature actually are operative in accelerated tests at higher temperatures.

Modulators
Modulators shape the optical beam. Almost all are electro-optic devices in which an electrical signal is used to change the refractive index of the optically non-linear material of which the waveguide is made. Electro-optic switches are closely related structures.

Wavelength Multiplexers, Selectors, and Isolators
Wavelength multiplexers combine two or more optical signals into one, so that many can be carried by a single waveguide, even at the same time. Diffraction gratings are extensively employed. Wavelength selectors, or de-multiplexers, reverse the process of the wavelength multiplexers, namely, to separate two or more optical signals out of one. Structures similar to those that do the multiplexing are used. Optical isolators block transmission of an optical signal. They are mostly magneto-optic devices.

Micro-optics (refractive and diffractive) and Coatings
Modern optical systems contain a variety of extremely small, passive structures such as lenses, gratings, and prisms that affect the optical signal by means of refraction or diffraction. These structures need to be inexpensive but very reliable. Very thin coatings are used in many optical structures to control reflections.

Connectors and Optical Alignment
Connectors mechanically align and hold an optical fiber to another optical structure, usually in a manner that is expected to be repeatedly demounted many times as opposed to permanent or semi-permanent fixing as done in alignment below. One such connector is seen in Figure 1. Typically, the fiber is fixed inside a ceramic collar called a ferrule which mates with another structure.

Optical alignment is the process or processes for aligning and holding bare fibers or waveguides in place with respect to other optical structures. This enables efficient transmission of an optical beam. Because of angle-of-acceptance reasons, optical systems are much more susceptible to micrometer and submicrometer dimensional errors than are electrical. Two general alignment methods are used, active and passive. Active alignment involves moving the fiber end with respect to the structure to which it is to be aligned until the light signal is maximized at which time the fiber is fixed. Passive alignment involves fixing fibers into prealigned mechanical guides such as grooves. Of the two, passive alignment is less expensive, but also less reliable.

Substrates
Substrates primarily provide a mechanically rigid base for other electronic or optical structures in the module. Substrates can be very complex structures providing electrical power, signal, and ground to many other structures as well as providing paths for the escape of generated heat.

Die Attach
Die attach refers to the means whereby components such as lasers or detectors are affixed to the substrate and electrical connection is made. Solder and thermally conductive, polymeric adhesives are most common for attaching components to the substrate in optical modules. This is referred to as "direct chip attach (DCA)," even though optical structures are involved. Electrical signal connection is often done by means of wire bonding. Thermal control is especially important in optical modules primarily because the lasers are so sensitive to temperature changes. Currently, most designers rely upon modeling to predict the temperature distributions.

Die Encapsulant
Die encapsulants are used to cover the optical structures or modules to protect them from the environment. The encapsulant is almost always a thermosetting resin like an epoxy. The encapsulant can intrude into the optical paths and distort or crack the structures due to differential thermal shrinkage.

SUCCESS FACTORS

Optical Waveguides
The primary gaps in the data on materials include thin-film versus bulk properties, effective index, optical loss due to material scattering as function of wavelength, waveguide loss (for both planar and channel waveguides) as function of temperature, and moisture absorption. A special data need is correlating loss to impurities.

Metrology needs include ways of measuring the dimensions of surfaces and interfaces, mapping any spatial variations of the refractive index or the birefringence, and detecting optical degradation with temperature. It was noted that the roughness of the walls of a waveguide affects its performance, so any metrology for the dimensions of surfaces and interfaces should include the physical condition or roughness of a buried sidewall as well as an external surface. A particular need is to standardize launch conditions into waveguides whose responses or properties are being measured.

Sources and Detectors
A particular metrology need for sources is a means of measuring the optical properties, especially absorption, of the substrate as a function of impurity/dopant concentration. This is especially important for substrates that are intentionally doped to make them semi-insulating. Calibrated linear sources were an identified need. Closely related is the need for standard measurement methods for optical power of a source as function of solid angle.

Extensive discussions took place on problems associated with the effects of the metallurgy used to do DCA of sources to substrates and those requiring soldering in general on the sources themselves. However, no consensus was reached on any specific recommendations for either metrology or data for further understanding. Copper was mentioned as possibly inducing stress in sources and some means for directly measuring soldering-induced interfacial stresses was suggested.

A data need for detectors is understanding the material parameters that control "dark current" that flows when the detector is not illuminated. In addition, measurements of the sensitivity or absorption profile of the photodiode, both laterally over its face and vertically as a function of depth, and standard measurement techniques for characterizing electrical crosstalk between detectors in an array are needed. Appropriate data are especially needed on which to base accelerated life tests for detectors. Calibrated linear sources would be useful in this regard.

Modulators

Standard measurement techniques and data on the complex dielectric constant of thin layers as a function of electrical frequency are needed. Standardized configurations for measuring the electro-optic coefficient as a function of electrical frequency and optical wavelength are required. A special metrology need is standard techniques for measuring the overlap of electrical fields or "field mapping." Current modulator materials are susceptible to damage and degradation simply due to the propagation of the optical signal. Means for measuring optical damage threshold are desired. No consensus exists on a quantitative definition of "optical damage threshold."

Wavelength Multiplexers, Selectors, and Isolators

The main metrology need for multiplexers is the ability to verify what has been produced in manufacture. For this purpose, standardized techniques for measuring the dimensions of the structures with submicrometer precision and calibrated wavelength standards are needed. These same needs exist for selectors as well. Consensus was reached that dispersion is a concern only in the case of high bandwidth multiplexers and demultiplexers. For this, calibrated wavelength standards over a wide range of frequencies would be extremely important. The principal need for optical isolators is a standardized technique for precision measurement of the magneto-optic coefficient.

Micro-optics (refractive and diffractive) and Coatings

Data on refractive index as function of temperature and wavelength, metrology and data on thin-film versus bulk properties, and metrology for characterizing the physical and chemical conditions of surfaces and interfaces are important for micro-optics. In addition, metrology is needed for measuring stress in micro-optic structures that typically arise from the processing of the module. Thin-film metrology is especially important for advanced thinner coatings. Recent work indicates values of some properties of thin coatings can differ by orders of magnitude from values seen in thicker coatings or bulk form. Metrology for characterizing the physical and chemical condition of the surface onto which the coatings are applied and measuring the adhesion of the coating to the substrate are important.

Connectors and Optical Alignment

The main need for connectors is techniques for measuring the thin-film bonding strength between the fiber and the ferrule. In the case of optical alignment, data are needed on factors that control the coupling efficiency as a function of time and temperature. Japanese experts handle this problem simply by using stronger light sources and beam-expanding optics so that the system will continue to operate despite alignment drift. Measurement of modal noise is also needed.

Substrates

The following substrate issues are especially important to optical interconnection.

- Thin-film metrology
- Precision measurement of dimensions and dimensional metrology standards
- Metrology for surface analysis and characterization for physical (e.g., roughness) and chemical (e.g., contamination) conditions

Die Attach
Good thermal modeling requires good values of thermal conductivities and diffusivities, and other properties such as heat capacities and densities of materials. Reliable values are hard to come by due to the variety of materials involved and their morphologies. Thermal resistances of interfaces are especially hard to predict with any precision. Thus, techniques for experimentally mapping temperature distributions or experimentally assessing the thermal performance of optical structures and modules would be reassuring and welcomed to verify simulation tools. Thin-film thermocouples or the spectral shifts of the lasers' outputs were mentioned as two possible approaches. Thin-film thermocouples may also find use as possible early failure-warning sensors. Metrologies for accurate non-contact mapping of temperature at various points with high spatial resolution and for assessing the thermal resistance of various layers as a function of their morphologies were highlighted.

A special and yet not clearly understood problem is the effect of contaminants on optical components, such as lasers, from the die attachment process. Soldering flux is especially suspect in this regard. Further research is needed before clear metrology or data needs can be identified.

Die Encapsulant
Refractive index in addition to properties of general interest to polymers - such as CTE, glass transition temperature, elastic strength, and thermal conductivity and diffusivity - is important. Gaps identified included data for the refractive index and CTE, and metrology and metrology standards for refractive index and transmittivity, particularly in thick-film dielectrics.

RECOMMENDATIONS

Five major cross-cutting issues were identified pertaining to the optical components considered. Reflecting these issues, the following technical efforts, listed in decreasing priority, are recommended.

- **Metrology and data for thin films, especially of polymers**
- **Dimensional metrology, especially at the submicrometer scale**
- **Characterization of the physical and chemical conditions of surfaces and interfaces**
- **Expanded database of important material properties**
  For example refractive index, CTE, optical absorption, complex dielectric constant, adhesion - especially for thin films, and as a function of electrical frequency, optical wavelength and modulation frequency
- **Non-contact, spatially resolved temperature measurement**

Thermal and Mechanical

Ephraim Suhir, AT&T Bell Laboratories
David Read, NIST Materials Reliability

INTRODUCTION

The scope of the working group on thermal and mechanical properties was defined by considering industry's present and future use of material properties information on the thermal and mechanical behavior of commodity and advanced packaging and interconnect structures. These structures include plastic packages, various single- and multi-chip modules including SCM-Ls, MCM-Ls and MCM-Ds, printed circuit boards and flex, connectors, solders and solder joints, heat sinks, and optical and photonic interconnection structures. Material properties and data issues discussed were those relevant to design, manufacturability, and reliability; with specific attention to data needed for modeling and simulation of electronic devices during manufacture and in use. Little discussion took place on standards for manufacturability or reliability and device-level standards such as geometry, dimensions, numbers of pins, etc.

Product drivers such as low cost, short time-to-market, high reliability, and high functionality and performance were repeatedly stressed by industry. These drivers dictate profitability, apply to all product areas discussed during the technology-focused working groups, and are controlling factors in determining future technical work in thermal and mechanical property data and metrology. New markets such as hand-held/portable products and wireless high frequency applications will introduce new materials and design requirements. Consensus exists that accurate and cost-effective modeling and simulation is needed to meet these challenges.

Industry's ability to invest in the technology base needed to address these challenges is shrinking due to strong competitive pressures. Packaging and interconnection materials weakly impact system cost. They do, however, strongly affect product reliability. This, in conjunction with the pre-competitive nature of material data and measurements, acts to motivate collaboration among competitors.

SUMMARY

The American electronics industry needs, and does not yet have, comprehensive thermal and mechanical properties data to enable expanded reliance on modeling and simulation of products during manufacture and use.

A common inventory of thermal and mechanical properties is needed to support finite element modeling of package and interconnect designs. This encompasses data on polymers, metals, and ceramics.

Interfaces are ubiquitous throughout all levels of packaging and interconnection. No standard methods exist for measuring or modeling interfaces though numerous standard tests are employed for investigating adhesion. Needs exist to understand further the fundamentals of interfaces as well as modeling methods for predicting interface failure based on factors such as material properties or loading.

Significant improvements are needed in the availability and quality of existing properties data characteristic of materials - as well as structures - at the geometries, dimensions, and constraints found in assembled products.

Industry believes NIST can play an important role in materials metrology and standards for electronic packaging and interconnection. Specifically, it is suggested that NIST could:

- develop fundamental understanding of important electronic packaging materials;
- develop and disseminate measurement methods and procedures, not simply publish technical papers;
- work closely with standards setting bodies, such as ASTM, IPC, or SEMI;
- usher development of draft standards through appropriate technical societies; and
- produce standard reference materials.

PARTICIPANTS

Participants in this working group represented many of the leading U. S. electronics companies, including producers of final products, components, devices, and materials.

Coordinator: Ephraim Suhir, AT&T Bell Laboratories
Facilitator: David Read, NIST Materials Reliability

Members:
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William Chen, IBM Corp.
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G. Marinescu, Purdue University
John Mather, Rockwell International
Gregory McKenna, NIST Polymers
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Drew Nelson, Stanford University
Luu Nguyen, National Semiconductor
Ray Pearson, Lehigh University
Sharad Shah, Digital Equipment Corp.
Robert Sundahl, Intel Corporation
Minoru Taya, University of Washington
Clare Thiem, USAF Rome Laboratories
Walt Winterbottom, Ford Motor Company
Yiu-Man Wong, AT&T Bell Laboratories
Xin Wu, University of Maryland CALCE

STATUS AND ISSUES

Figure 2 shows the size and thickness scales of material elements found in various packaging and interconnect structures.

Modeling and Simulation
Key issues in design, manufacture, and service reliability can be addressed through accurate simulation of the thermal and mechanical behavior of packaging and interconnect structures. Simulations model the manufacturing process, which can be observed and controlled, and the reliability of products, even though the exact product use conditions are not fully known or controllable. Simulations typically utilize finite element analysis, FEA, although more general models based on acceleration factors are also used. Industry is adamant about the vital importance of thermal-mechanical modeling and that it be quantitatively accurate.

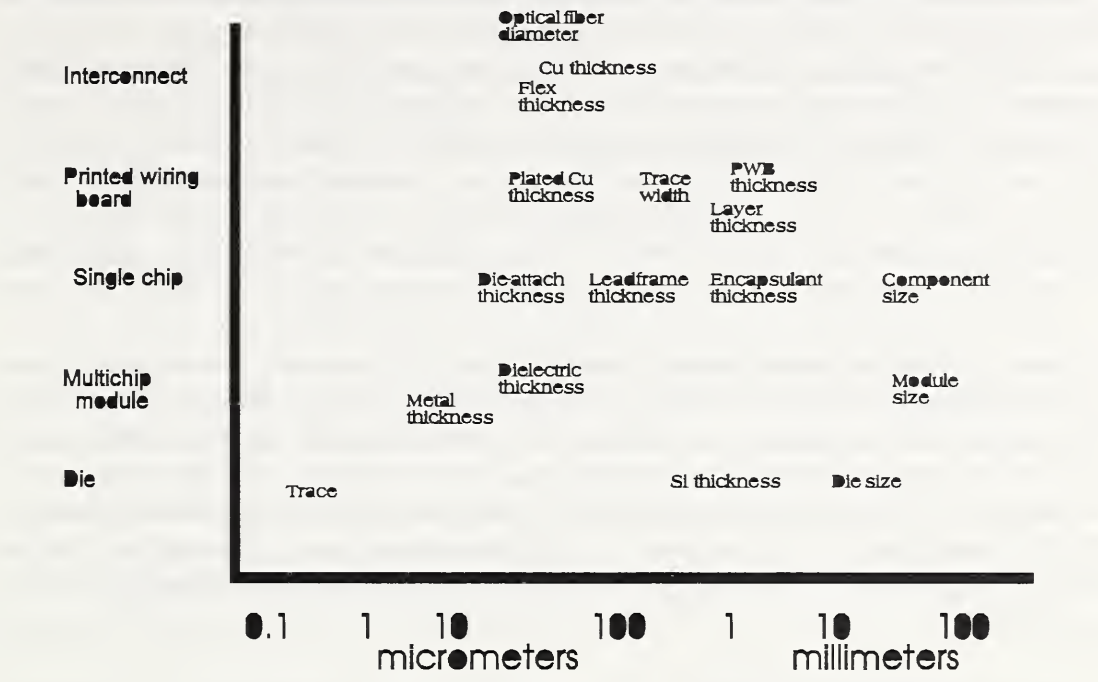
Simulation replaces a substantial portion of prototyping and test of actual devices. Simulation costs much less and is much quicker. Product-process trade-offs can be explored using simulation. Cost reductions brought about by the use of verified simulations have been demonstrated but the simulations of new advanced multilayer structures will not likely reach a level of accuracy where quantitative results are trustworthy unless there are reliable and applicable materials and processes databases.

The need for simulation of thermal and mechanical behavior applies to all materials systems and to all levels of packaging, although chip, component, and board level packaging are most directly applicable. Modeling requires relevant property values and must reflect the temperature range, moisture content, anisotropy, size scale, and thickness that is characteristic of the material found in the actual packaging or interconnect structure. Barriers to quantitative modeling are ascribed to:

- lack of accurate input data both on material properties and on details of structural geometry,
- lack of realistic treatment of important failure modes, such as interfacial delamination or fracture, and
- lack of physical understanding of the effect of manufacturing processes on materials properties and behaviors.

The role of manufacturing imperfections as latent failure sites is also not fully understood.

Figure 2: Typical Dimensions of Packaging and Interconnect Structures



Standardized Tests and Data

There are no standardized test procedures for measuring many of the thermal, mechanical, and moisture characteristics for very thin films, though many exist for bulk specimens. This lack of measurement standards is a major roadblock to appropriate material properties data and verifiable models. Users are often compelled to accept values provided by the materials supplier. A theme that emerged from time to time during the technology-focused discussions was the need for improved materials and materials systems, in addition to better materials metrology and data. The development of improved materials is outside the scope of this workshop, although improved metrology can lead to improved materials. Tools for measuring the local and global CTE of many different types of structures are needed. This information is needed for design, models of reliability, and for verification of presently used modeling tools. Data on materials both as a function of temperature and moisture content are required.

Polymer Issues

Materials such as diebond adhesives, molding compounds, and underfill encapsulants, while nominally known as polymers, are highly filled composites to optimize their functional properties.

Data on polymers, even on bulk specimens, are often not available for many of the specialized polymers used in electronic packaging structures. Polymer resins also typically contain fillers, which add another level of complexity to their behaviors. When used as molding compounds and encapsulants, non-linear responses such as the variation of modulus with temperature are important. An understanding of the variability in material properties with conditions, such as specimen thickness, moisture content, temperature, or age is generally lacking.

Material properties are strongly dependent on processing, history, and environment. Consequently, handbook values of properties are inherently inapplicable. Actual behaviors must be verified by the user. Perhaps one of the most important issues is performance variability and tolerances. Device designs utilize some typical material property. Products that incorporate materials exhibiting this typical value perform as expected. Products that incorporate materials exhibiting atypical values can fail. In other words, establishing tolerances and preventing "outliers" becomes critical. The range of values for many performance characteristics of polymers is wider than for more familiar materials such as metals. The manufacture and reliability implications of "outliers" is not fully understood for polymers in packaging.

Polymer mechanical properties are time-dependent. For example, viscoelasticity is a rate-dependent phenomenon whereas modulus can be age-dependent as well as cure-dependent. Rate dependencies are considered in relation to the duration of a process, such as resin injection time. For example, resin processability is linked to the rheology of the material and, under certain circumstances, to wetting characteristics. Both of these factors are rate-dependent. Age dependencies are presently believed to have only weak effects on long-term reliability, the exception being reliability of interfaces.

Unexpected Faults and Failures

During manufacture, problems often arise for which ready explanations may not be available. A current example is the "popcorn" problem encountered during rapid heating. Moisture in the chip encapsulant expands during reflow soldering and damages the encapsulant and interfaces. When failures like this arise, it would be advantageous to have ready access to reliable material properties data, such as mechanical, thermal, and moisture properties. This would reduce the time needed to commence corrective action.

Military *versus* Commercial Reliability Standards and Mechanical Specifications

The influence of military specification and reliability standards in the manufacturing of commercial electronic products often arises during discussions of electronic packaging. Discussion related to military standards was not within the scope of this workshop. Standard measurement methods for materials testing and a basic understanding of materials behavior are believed suitable for pre-competitive collaboration but tests and test procedures for products should be the responsibility of individual companies.

SUCCESS FACTORS

Standard Test Procedures

Standard test methods for materials as used in electronic packaging and interconnect structures are needed as expressed by the working group participants. This also includes standard test procedures and structures for the material of interest. Contrary to bulk materials, thin film specimens for packaging materials formed *in situ* cannot be extracted from large pieces of the material and mounted in a testing machine for measurement.

Standard Reference Materials
For each standard test method comes the need to verify the procedure by using standard reference specimens for which the right answer is known. Participants believe that developing and making standard reference materials (SRM) available to industry is an important NIST activity and believe that a mechanism whereby industry priorities for SRMs would guide NIST activities in new SRM development is an important ingredient for success.

Materials Databases
Readily available and comprehensive materials property data are needed. There are presently several data bases for material property information. Consensus exists that such data bases need not contain data on materials produced under unique manufacturing conditions. Instead, data bases should strive to archive "baseline" material characteristics. Universities are the principal data generators, assemblers, and keepers, although individual firms also maintain their own proprietary and non-proprietary databases. However, universities can create new data only slowly and generally do not have the resources to verify data extracted from the literature and included in databases. NIST's stability and impartiality as a government agency were considered big advantages for NIST as a data keeper.

Metrology for Manufacturing
Materials metrology is needed throughout the entire manufacturing process, from research and design to process development and process control. Metrology supporting research and design, where material behavior under varying conditions is carefully explored and documented, may be the purview of the university, government laboratory, industrial research environment. Process development requires simpler robust techniques so that specific materials can be evaluated under the varying conditions that might arise during manufacture. Process control measurements must be nondestructive, rapid, and not disruptive to the process.

RECOMMENDATIONS

The American electronics industry needs, and does not yet have, comprehensive thermal and mechanical properties data to enable expanded reliance on modeling and simulation of products during manufacture and use. Manufacturing and assembly processes require high-temperature excursions with polymers subjected to temperatures up to 300 °C in many cases. Under in-use conditions, transient stresses result from thermomechanical loading, vibrations, or shock when products are dropped or impacted.

A common inventory of thermal and mechanical properties is needed to support finite element modeling of package and interconnect designs. This encompasses the following data on polymers, metals, and ceramics.

- **Thermal**
  Coefficient of Thermal Expansion, CTE
  Thermal Diffusivity; Heat Capacity, and Thermal Conductivity
  Glass Transition Temperature (for polymers)
  Polymer Viscosity

- **Mechanical**

Stress-Strain:	tensile, bulk, and shear elastic moduli
	Poisson's ratio
	tensile and compressive stress-strain relationships
	tensile and compressive yield, and ultimate strengths
	ductility and elongation to failure
Fracture Toughness:	polymers, plated copper, solder, polymer-copper and polymer-glass interfaces, silicon, GaAs, alumina, ceramics
Fatigue:	thermomechanical (strain-controlled and low cycle)
	vibrational (external loading controlled and high cycle)
Adhesion:	linked to interfacial fracture toughness and strength
Stress:	residual and thermal stresses
	stress concentrations (edges and corners)

- **Moisture**

  Location, content, diffusivity, and saturation
  Effect on mechanical properties

Interfaces are ubiquitous throughout all levels of packaging and interconnection. Interfaces and adhesion were emphasized on many occasions during the workshop. No standard methods exist for measuring or modeling interfaces though numerous standard tests are employed for investigating adhesion. Needs exist to further understand the fundamentals of interfaces as well as modeling methods for predicting interface failure based on material properties, loading, etc.

To improve upon the quality of existing properties data, characteristics of materials - as well as structures - at the geometries, dimensions, and constraints found in assembled products are needed. Thin layers formed *in-situ* can exhibit properties that are different from those of bulk specimens nominally composed of the same material. The property differences arise from differences in microstructure and chemical composition. For example, vapor-deposited aluminum metallization can have very small grains, and can contain impurities not present in the starting material.

Industry believes NIST can play an important role in materials metrology and standards for electronic packaging and interconnection. Specifically, it is suggested that NIST:

- develop fundamental understanding on materials important in electronic packaging;
- develop and disseminate measurement methods and procedures, not simply publish technical papers;
- work closely with standards setting bodies, such as ASTM and IPC;
- usher development of draft standards through appropriate technical societies; and
- produce standard reference materials.

A specific concern is the slow pace at which standards are developed and accepted through existing organizations. A multitude of improved standards are needed. It is suggested that NIST could establish in conjunction with existing organizations a task group to address standards related issues and utilize frequent teleconference and face-to-face meetings to accelerate the pace of progress. A goal of this activity should be to produce measurement standards which are developed and validated with industry.

PHYSICAL, CHEMICAL, AND INTERFACES

Chung Lee, MCC
Brian Dickens, NIST Polymers

INTRODUCTION

The working group on physical, chemical, and interface properties organized the relevant issues from the technology-focused working groups into the matrix shown in Table V. Time limitations prevented a wide range discussion of all these topics. Instead it focused mainly on polymers and polymeric interfaces. Solders, ceramics, optical interconnections, and other types of interfaces were not well discussed.

Table V: Physical, Chemical, and Interface Issues in Electronic Packaging

TECHNOLOGY	PHYSICAL	CHEMICAL	INTERFACES
SINGLE CHIP	Rheology, Moisture absorption, desorption, & concentration profile	Outgassing, Solvent compatibility	Adhesion (rigid/rigid, plastic/rigid)
MULTICHIP, HYBRID, FLAT PANEL DISPLAY	Thin film properties, Anisotropic properties, Thermal conductivity	Cure monitoring, Cure shrinkage	Delamination, Adhesion mechanism, Stress concentration
PRINTED WIRING BOARD, FLEX	T_g, CTE, Moisture Content	Cure and Properties interrelationships, Cure variability	Glass/metal/resin adhesion
ELECTRICAL & OPTICAL INTERCONNECTION AND ASSEMBLY	Viscoelastic properties	----	Solderability

SUMMARY

Physical, Chemical, and Interfacial considerations are pervasive to all packaging and interconnection materials and structures. Testing and metrology are needed to satisfy four different constituencies. Designers need material properties for computerized modeling. Assemblers need quality control measures. Manufacturers need to make decisions about whether to manufacture new products using new materials or use new processes. Product life-prediction methods are needed. Life prediction is a constantly recurring problem and is an area where it is easy to make fallacious assumptions.

Research, development, and/or implementation efforts are needed in five key technical areas:

- Testing and metrology
- Standards
- Interfaces and adhesion
- Moisture measurement and control
- Information exchange by round robin

To help catalyze activities in the above areas, it is suggested that NIST could:

- Spearhead a national task force on metrology
- Conduct a review of existing test methods used by the industry and identify new standards needs
- Assist industry in developing improved affordable testing methods
- Utilize industry round robins for developing and disseminating expertise
- Make available NIST services and facilities
- Highest priority technical challenges include interface and adhesion of polymer films on substrates, and moisture characterization, measurement, and assessment

This work should be conducted in concert with SEMATECH, IPC, OIDA, SRC, and Sandia National Laboratories. The IPC, OIDA, and SRC should lead industry in defining relevant test structures while Sandia should assist in fabricating test structures.

PARTICIPANTS

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John Jackson, SEMATECH
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Dennis Olsen, Motorola
Robert Shick, BF Goodrich
Larry Sparks, NIST Materials Reliability
Paul Townsend, Dow Chemical Co.
Yiu-Man Wong, AT&T Bell Laboratories
Tien Wu, IBM Corp.
Wen-Li Wu, NIST Polymers
Edward Yung, MCNC

STATUS AND ISSUES

A wide variety of materials is used in electronic packaging and interconnection. These materials must be characterized for use in designs and monitored in manufacture. Ceramics are much better understood than are polymers and their properties are more stable. Packaging and interconnection technologies are increasingly using polymeric materials because of desired properties, manufacturing ease and cost advantages. Polymers are formed with lower-technology procedures than ceramics. Polymers often do not exist in an equilibrium state and consequently their properties vary with history and environment, especially temperature and humidity. Many polymers, such as polyimides, exhibit numerous anisotropic characteristics.

Much of the data that is useful to a designer of electronic components is produced by the manufacturer of the components rather than by the suppliers of the materials. Each manufacturer obtains his own data. Manufacturers' data are currently considered to be proprietary and are not shared. Suppliers do not provide enough data because their materials are used in many configurations and, in their opinion, not enough demand exists to warrant extensive measurements for any one configuration or use. However, measurement techniques are much more generic and development of techniques benefits much of the industry. A realistic first step is to develop a database of measurement techniques. Generating a general database of material properties specific to the uses in electronic packaging will be more difficult and will first require a battery of measurement techniques.

Manufacturers tend to develop tests to reflect their specialized needs. Many of these tests are subjective, overly simple, inaccurate, and do not probe characteristics fundamentally related to failure modes or mechanisms. Conversely, measurement techniques made in research laboratories can be unrealistically expensive, time-consuming, and divorced from the particular problem of the manufacturer.

In research environments, numerous advanced tests are available. They include:

Physical
- Orientation - Small angle X-ray diffraction, FTIR
- Anisotropy - Birefringence, Differential capacitance, Photothermal measurements

Chemical
- Degree of cure - FTIR/ATR, Dielectric spectroscopy, Photoacoustic spectroscopy, Capacitance

Interfaces
- Interfacial toughness - Stress pulse, Confocal Microscopy, Micro-indentation

A diverse assortment of tests also exists in the manufacturing environment. Table VI illustrates the range of tests used for examining interfaces and adhesion.

Table VI: Characteristics of Adhesion Test Methods

TECHNIQUE	CORRELATION TO PERFORMANCE	UNCERTAINTY
Lead Pull	Medium	10-50%
Adhesive Tape	Poor	?
Lap Shear	Medium	20-30%
Stud Pull	Medium	20-30%
Hook Pull	Good	<10%
Ball Shear	Good	<10%
Interfacial Toughness	Good	15%
Micro-indentation	Good	?
Wetting Balance	Medium	>50%
Area of Spread	Medium/Poor	>50%
Keyhole Capillary	Medium	?
Capillary Rise	Good	<10%

SUCCESS FACTORS

Testing and Metrology

Material properties that fall within the scope of this working group and that warrant the development of improved testing and metrology are listed in Table VII. Primary needs are extensive tests, particularly *in-situ* tests, and data for orientation in thin films, anisotropy in CTE, thin film interfaces, moisture at interfaces, microscopy of fractured surfaces, interfacial fracture toughness - separated according to whether mode I or mode II or mixture - and for rigid/rigid and plastic/rigid laminates in micro-dimensions. Tests for reliability require considerable improvement in reproducibility and sensitivity. Accelerated testing requires better linkage with known failure mechanisms to weed out fallacious assumptions and inappropriate acceleration mechanisms.

Table VII: Material Properties Requiring Improved Metrology

Degree of cure	Viscosity
Cure shrinkage	Outgassing
Water diffusion and solubility	Glass transition temperature
Compatibility with solvents	Thermal conductivity
Anisotropy	Coefficient of thermal expansion

Standards

Standard industry testing methods should be developed that produce numeric results either through direct measurement or by counting statistics, instead of producing a pass or fail result. This shift to numeric results will facilitate easier process control and optimization. Standard testing methods must be easy to carry out and must provide means by which precision and accuracy can be assessed.

Standard reference materials that exhibit the following characteristics are needed:

PHYSICAL
- Anisotropy/orientation
- Viscoelasticity
- Dimensional stability
- Permeability of water
- CTE (x,y vs. z)
- T_g

CHEMICAL
- Degree of cure
- Moisture content and distribution in thin polymer films and at interfaces

INTERFACE
- Fracture toughness

Interfaces and Adhesion

Adhesion depends on material properties and on the geometry of the interface. Techniques for measuring the adhesive strength of an interfacial bond must accommodate a wide range of materials and specimen sizes. They should quantify the local characteristics and rely on *in situ* measurements. Generic test structures are needed to simulate geometries and configurations. NIST may be particularly suited for developing techniques given that industry often cannot invest in these generic programs.

Adhesion tests currently do not distinguish failure modes and consequently mix delamination mechanisms. A better fundamental understanding of interfaces and adhesion, as well as better sensitivity and applicability of current tests is needed. Data are needed as a function of moisture and perhaps other common contaminants at the interface. Measurements should be made *in-situ* as much as feasible. Tests are needed which unambiguously determine peel and shear strengths at interfaces such that they can be related to the finite element modeling interface simulations. Interfaces of particular concern are listed in Table VIII.

Improved solderability tests and tests are needed for predicting solderability during manufacture. This will require an increased understanding of the reactions occurring at the interface during the soldering process. Interface reactions which deplete tin in solder and cause failure of solder joints need to be characterized.

Table VIII: Key Material Interfaces

Polymer*/Silicon	Metal/Solder
Polymer*/Polymer*	Metal/Silicon
Polymer*/FR4	Metal Wire/Metal pad
Polymer*/Metal	Metal/Optical fiber
Polymer*/Ceramic	III-V Semiconductors/All materials
Polymer*/Glass	

* Polymer types include epoxies, polyimides, and fluoropolymers.

Moisture
Moisture weakens polymeric materials, raises the dielectric constant, induces corrosion, and causes "popcorning" - an effect in which components are damaged by the sudden generation of vapor as the component is heated. *In-situ* moisture tests, improved understanding of the mode of water-uptake, and mechanisms of moisture-induced failures are needed.

Information Exchange
Information exchange and dissemination is a continuous problem due to continual updating of information, availability of new materials, and inevitable changes in key personnel. Round robin exercises were felt by industry to be an especially efficient method for information exchange and dissemination. Round robins have the virtues of exchanging generic know-how and of focussing research efforts to reflect industry constraints and standards.

RECOMMENDATIONS

Industry believes NIST is well positioned to exert leadership in the following ways:

- Spearhead a national task force on metrology
- Conduct a review of existing test methods used by the electronics industry to identify appropriate new standards
- Assist industry in developing improved affordable testing methods
- Utilize industry round robins for developing and disseminating expertise
- Make available NIST services and facilities
- Highest priority technical challenges include interface and adhesion of polymer films on substrates, and moisture characterization, measurement, and assessment

In addition, the working group suggests that strong collaborations between NIST and other organizations occur to take advantage of individual capabilities and strengths. For example, cooperation between NIST and SEMATECH will benefit U.S. manufacturers. The working group also believes that IPC, OIDA, and SRC should lead industry to define appropriate test structures while the national labs, such as Sandia, be utilized to fabricate test structures.

APPENDIX A: AGENDA

Thursday, May 5

7:30am Registration

8:00am Introduction
Michael Schen, Workshop Chairman
NIST

8:05am Welcome
Lyle H. Schwartz, Director
NIST Materials Science and Engineering Laboratory

8:20am Keynote Address
Arati Prabhakar, Director
United States Department of Commerce
Technology Administration
National Institute of Standards and Technology

8:45am *Materials Challenges in Microelectronic Packaging and Interconnection*
Barry Johnson, Director, Core Technologies,
Motorola

9:30am *Emerging Applications for Low Cost Optoelectronics*
Paul Haugsjaa, Network Technologies Laboratory,
GTE Laboratories

10:15am Break

10:30am *Materials Metrology and Data for Design, Manufacture and Reliability Analysis*
Che-Yu Li, Director, Materials Science and Engineering,
Cornell University

11:15am Technology Roadmap Reports
Semiconductor Industry Association (SIA)
John Kelly, Director, Manufacturing Systems / Packaging Sciences,
Semiconductor Research Corporation

Institute for Interconnecting and Packaging Electronic Circuits (IPC)
David Bergman, Director, Technical Programs,
IPC

Optoelectronics Industry Development Association (OIDA)
Davis Hartman, Manager, Optical Interconnect - Optical Communications
Motorola Inc.

Thursday, May 5 (continued)

12:00pm Lunch

1:00pm Charge to Working Groups

1:10pm Working Session I: Metrology and Data for the Design, Manufacture and Reliability Assessment of Critical Structures and Processes

i) Single Chip
William T. Chen, IBM - Coordinator
G. Thomas Davis, NIST Polymers - Facilitator

ii) Multichip Module, Hybrid, and Flat Panel Display
Luu T. Nguyen, National Semiconductor - Coordinator
Aime DeReggi, NIST Polymers - Facilitator

iii) Printed Wiring Board and Flex
Rolland Savage, Gould, Inc. - Coordinator
Bruno Fanconi, NIST Polymers - Facilitator

iv) Electrical and Optical Interconnection and Assembly
Greg Munie, AT&T Bell Laboratories - Coordinator
Carol Handwerker, NIST Metallurgy - Facilitator

3:00pm Break

3:15pm Working Session I (continued):
Prepare Reports

5:10pm Plenary Session - Reports of Working Groups and Discussion
Challenges in Design, Manufacture, and Reliability Assessment

6:15pm Adjourn for the Day

6:30pm Reception and Banquet

8:00pm *Electronics R&D Activities Across the Federal Government*
Lance Glasser, Chairman, Electronic Subcommittee
National Science and Technology Council
Advanced Research Projects Agency

Friday, May 6

7:30am Breakfast Meeting
(Workshop Steering Committee)

8:00am *Technology Partnerships*

Semiconductor Research Corporation, SRC
John Kelly, Director, Manufacturing Systems / Packaging Sciences

Interconnection Technology Research Institute, ITRI
Marshall Andrews, Chief Executive Officer

National Institute of Standards and Technology, NIST
Michael Schen, Materials Science and Engineering Laboratory

9:00am *The NIST Advanced Technology Program - Latest Status*
John Gudas, Materials Program Manager
NIST Advanced Technology Program

9:30am *Administration Program to Enhance the Competitiveness of the U.S. Packaging and Interconnection Industry*
Nicholas Naclerio, Electronics Systems Program Manager
Advanced Research Projects Agency

10:00am Charge to Working Groups

10:15am Break

10:30am Working Session II: Metrology and Data for Electrical and Optical Packaging and Interconnection Materials and Material Structures

i) Electrical
Eric Bogatin, Sun Microsystems - Coordinator
Roger Marks, NIST Electromagnetic Fields - Facilitator

ii) Optical
Davis Hartman, Motorola Inc. - Coordinator
Joseph Carpenter, NIST Ceramics - Facilitator

iii) Thermal and Mechanical
Ephraim Suhir, AT&T Bell Laboratories - Coordinator
David Read, NIST Materials Reliability - Facilitator

iv) Physical, Chemical, and Interfaces
Chung Lee, MCC - Coordinator
Brian Dickens, NIST Polymers - Facilitator

Friday, May 6 (continued)

12:00pm	Lunch
1:00pm	Working Session II (continued): Prepare Reports
3:30pm	Break
3:45pm	Plenary Session - Reports of Working Groups and Discussion *Future Progress in Materials Metrology and Data*
5:00pm	Adjournment

APPENDIX B: PARTICIPANTS

Final Participants List
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May 5-6, 1994

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